LCFC Confidential

G Project M/B Schematics Document

AMD FP4 Bristol Ridge and Stoney Ridge SOC with DDRVI

AMD R16M-M1-30

2015-06-06

REV:1.0

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Title	Cover Page	
Size Custom	Document Number CG516	Rev 1.0
Date: Tuesday, April 12, 2016	Sheet 1 of 51	

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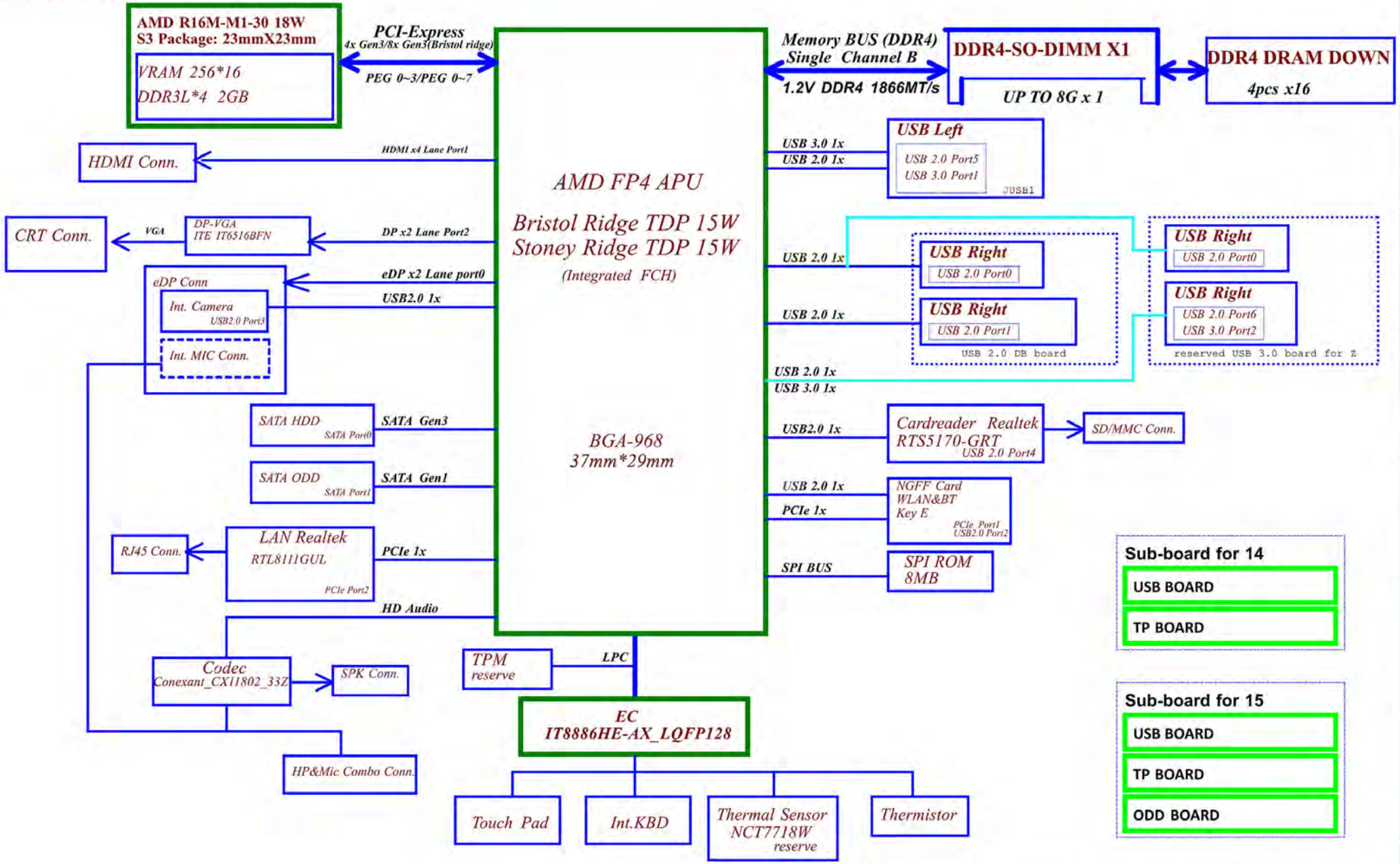

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Title: Block Diagram

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Date: Tuesday, April 12, 2016 | Sheet 2 of 51

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Voltage Rails (O --> Means ON , X --> Means OFF)

State \ power plane	B+ (+20VSB) +3VL +5VLP	+5VALW +3VALW (+3VALW_APU) +1.8VALW +0.95VALW +0.775VALW	+1.2V (+VSYSMEM_APU)	+5VS +3VS +1.8VS +1.5VS +0.95VS +0.6VS +2.5VS +APU_CORE +APU_CORE_NB +APU_GFX +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

DRAM Config.	BOARD_ID0 APIO8	BOARD_ID1 AGPIO10	BOARD_ID2 AGPIO16 internal pull up 40K
	0: 14''	0: Dis	0: No KBL
	1: 15''	1: UMA	0: KBL

USB Port Table

USB 2.0	USB 3.0	Port	ST Port device	BR Port device
EHCI0		0	RIGHT USB (2.0)	RIGHT USB (2.0)
		1	RIGHT USB (2.0)	N/A
		2	Blue Tooth	Blue Tooth
		3	Camera	Camera
xHCI	0	4	Card Reader USB 2.0 bus	Card Reader USB 2.0bus
	1	5	LEFT USB (3.0)	LEFT USB (3.0)
	2	6	N/A	RIGHT USB (3.0)
	3	7	N/A	N/A

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
ME@	Connector
14@	For 14" part
15@	For 15" part
EMC@	EMC Part
EMC_NS@	EMC reserve Part
EMC_14@	EMC 14 part
EMC_15@	EMC 15 part
RF@	RF Part
RF_PXNS@	RF GPU reserve part
UMA@	UMA SKU ID part
PX@	Discrete GPU SKU part
EXO@	EXO GPU Part
TOPAZ@	TOPAZ GPU Part
TPM@	TPM part
KBL@	keyboard backlight part
HDT@	HDT Debug part
BR@	Bristol Ridge Part
ST@	Stoney Ridge part
BRPX@	Bristol Ridge Discrete Part
S4GX4@	X76 SAMSUNG 2G
M4GX4@	X76 MICRON 2G
H4GX4@	X76 HYNIX 2G
S2G@	SAMSUNG 2G
M2G@	MICRON 2G
H2G@	HYNIX 2G
HDMI@	HDMI Logo

VRAM

SMBUS Control Table

X

	SOURCE	GPU	BATT	IT8586E	SODIMM	WLAN	Thermal Sensor	APU	Charger	PMIC	Vcore VR	GFxcore VR
EC_SMB_CK0 EC_SMB_DA0	IT886H +3VL	X	X		X	X	X	X	X	V	X	V +3VALW
EC_SMB_CK1 EC_SMB_DA1	IT886H +3VL	X	V		X	X	X	X	V	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT886H +3VS	V +3VS_VGA	X		X	X	V	V 1.8VS	X	X	X	X
EC_SMB_CK3 EC_SMB_DA3	IT886H +3VALW	X	X		X	X	X	X	X	X	V	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V	V	X		X	X	X	X

PCIE PORT LIST

	Port	Device	
GPP	0	N/A	
	1	WLAN	
	2	LAN	
	3	N/A	
GFX	0	ST GPU	BR GPU
	1		
	2		
	3		
	4	N/A	
	5		
	6		
	7		

EC SM Bus0 address

Device	Address
PMIC	?
GFxcore VR	?

EC SM Bus1 address

Device	Address
Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
Thermal Sensor	1001_100xb(reserve)
GPU	0x41(default)
APU SB-TSI	releate to F3x1E4[SbiAddr] or Address Select Pins setting

EC SM Bus3 address

Device	Address
Vcore VR	?

APU SM Bus address

Device	Address
DDR4 SO-DIMM	?
WLAN	RSVD

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Title: Notes List

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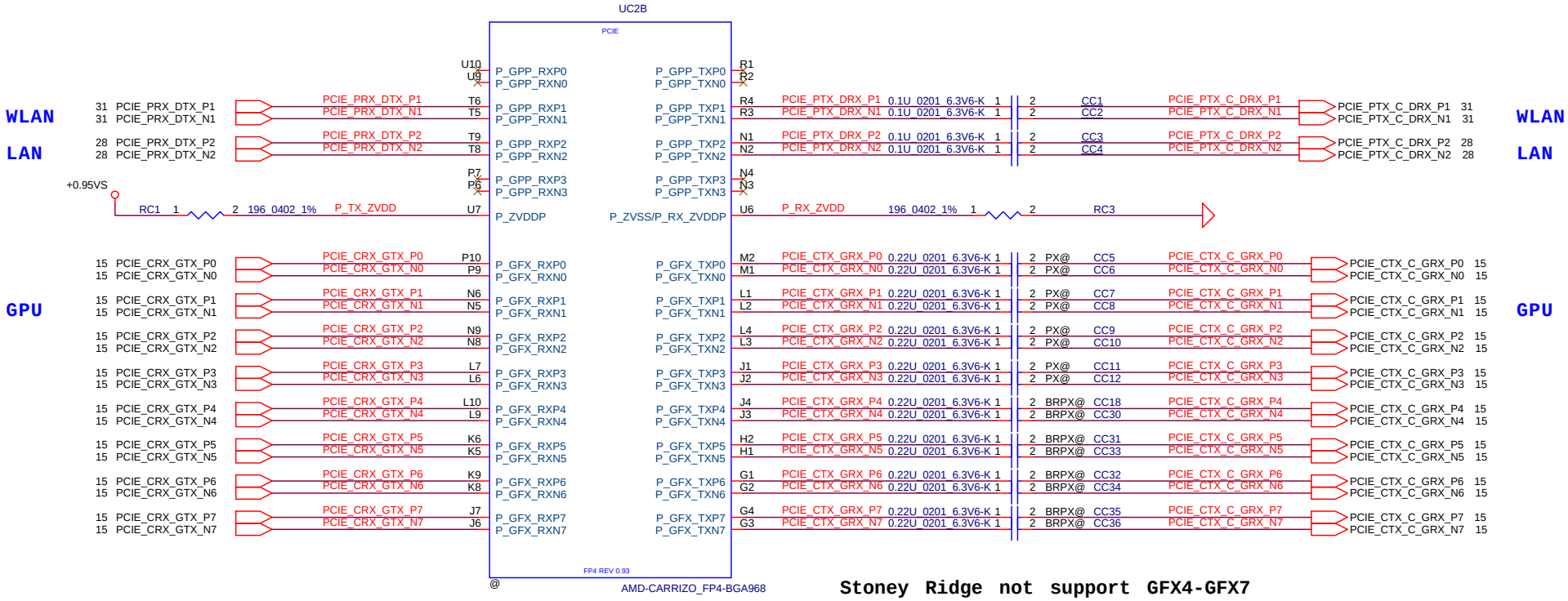
Date: Tuesday, April 12, 2016 | Sheet 3 of 51



Stoney Ridge not support GFX4-GFX7

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Title: *FP4 (PCIE I/F)*

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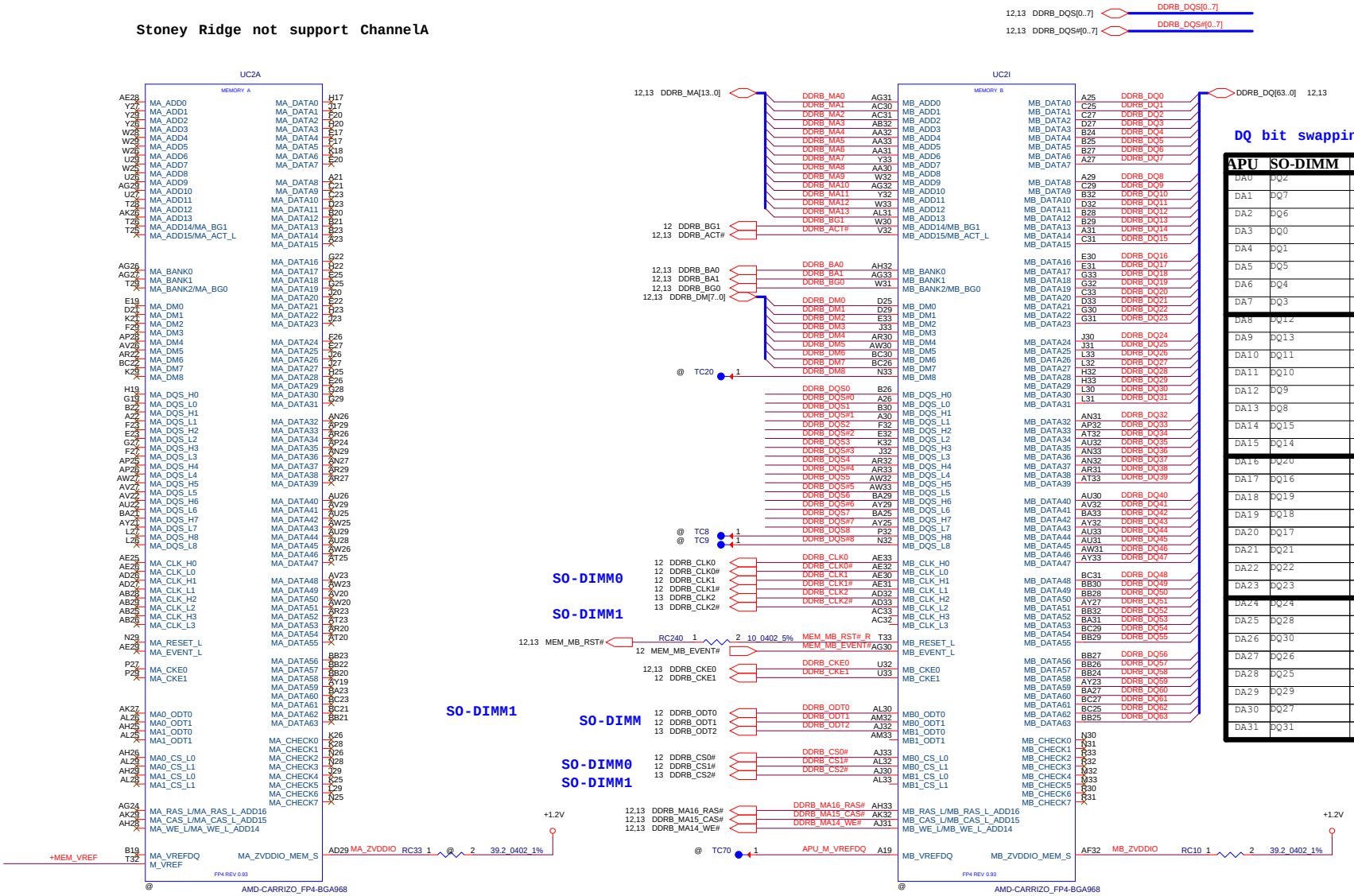
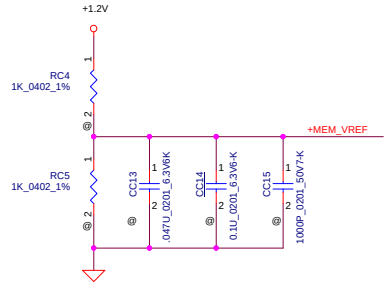
Stoney Ridge not support ChannelA

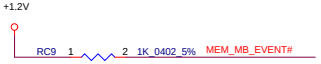


DQ bit swapping is allowed in a byte lane.

APU	SO-DIMM	DRAM
DA0	DQ2	UD1.0
DA1	DQ7	UD1.3
DA2	DQ6	UD1.4
DA3	DQ0	UD1.5
DA4	DQ1	UD1.2
DA5	DQ5	UD1.7
DA6	DQ4	UD1.1
DA7	DQ3	UD1.6
DA8	DQ12	UD1.11
DA9	DQ13	UD1.9
DA10	DQ11	UD1.12
DA11	DQ10	UD1.14
DA12	DQ9	UD1.13
DA13	DQ8	UD1.15
DA14	DQ15	UD1.8
DA15	DQ14	UD1.10
DA16	DQ20	UD2.7
DA17	DQ16	UD2.3
DA18	DQ19	UD2.4
DA19	DQ18	UD2.1
DA20	DQ17	UD2.0
DA21	DQ21	UD2.2
DA22	DQ22	UD2.6
DA23	DQ23	UD2.5
DA24	DQ24	UD2.9
DA25	DQ28	UD2.11
DA26	DQ30	UD2.12
DA27	DQ26	UD2.8
DA28	DQ25	UD2.13
DA29	DQ29	UD2.15
DA30	DQ27	UD2.14
DA31	DQ31	UD2.10

APU	SO-DIMM	DRAM
DA32	DQ39	UD3.1
DA33	DQ36	UD3.6
DA34	DQ35	UD3.2
DA35	DQ34	UD3.7
DA36	DQ37	UD3.5
DA37	DQ32	UD3.3
DA38	DQ38	UD3.4
DA39	DQ33	UD3.0
DA40	DQ45	UD3.15
DA41	DQ44	UD3.9
DA42	DQ47	UD3.14
DA43	DQ46	UD3.8
DA44	DQ40	UD3.13
DA45	DQ41	UD3.11
DA46	DQ43	UD3.12
DA47	DQ42	UD3.10
DA48	DQ55	UD4.0
DA49	DQ49	UD4.3
DA50	DQ54	UD4.2
DA51	DQ48	UD4.7
DA52	DQ53	UD4.5
DA53	DQ52	UD4.1
DA54	DQ50	UD4.6
DA55	DQ51	UD4.4
DA56	DQ61	UD4.14
DA57	DQ56	UD4.10
DA58	DQ63	UD4.11
DA59	DQ58	UD4.12
DA60	DQ60	UD4.13
DA61	DQ57	UD4.9
DA62	DQ59	UD4.15
DA63	DQ62	UD4.8





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Title: **FP4 (MEM)**

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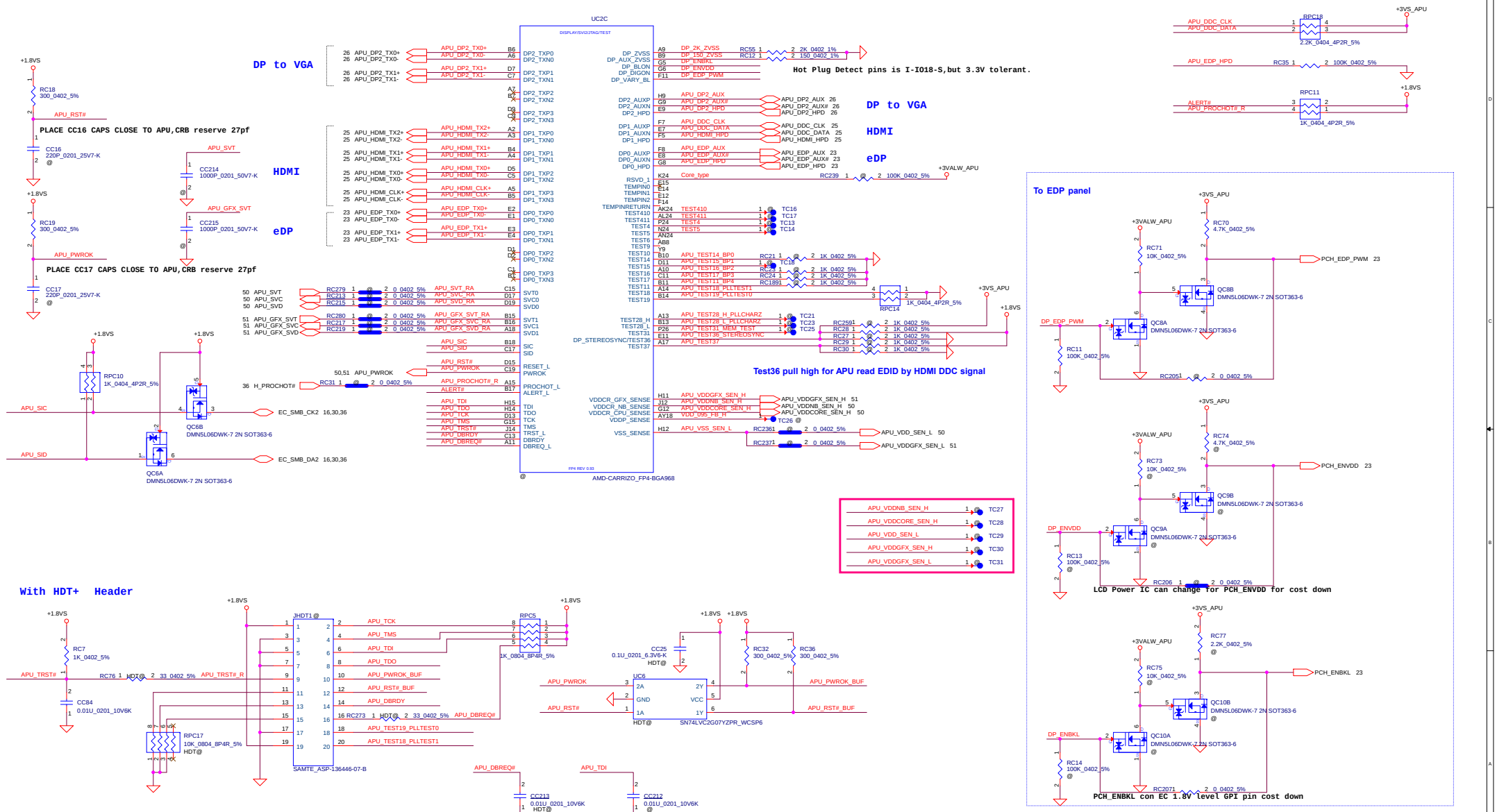

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Title: FP4 (DISPLAY/CLK/MISC)

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Date: Tuesday, April 12, 2016 | Sheet 6 of 51

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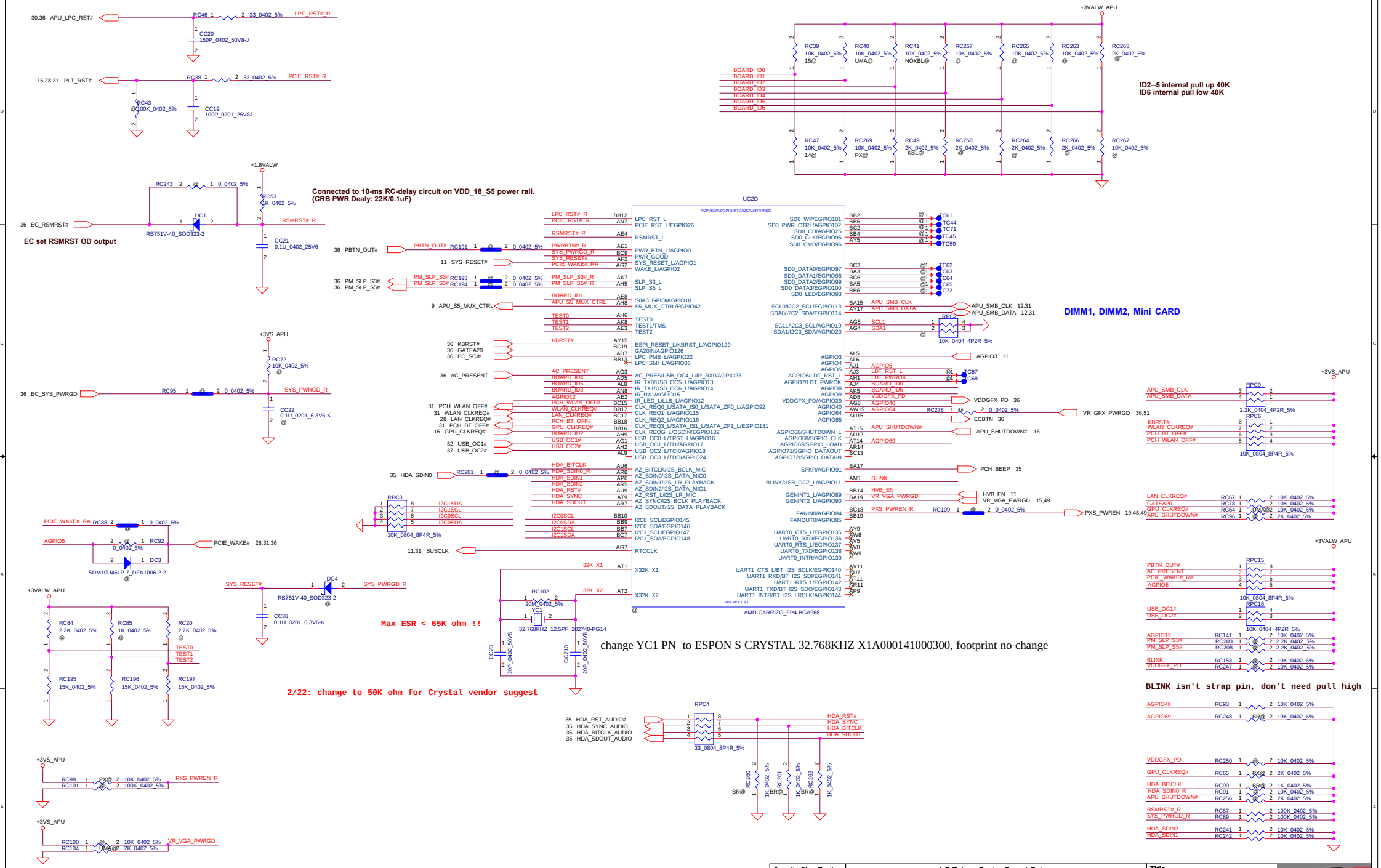

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Title: FP4 (GEVENT/GPIO/SD/AZ)

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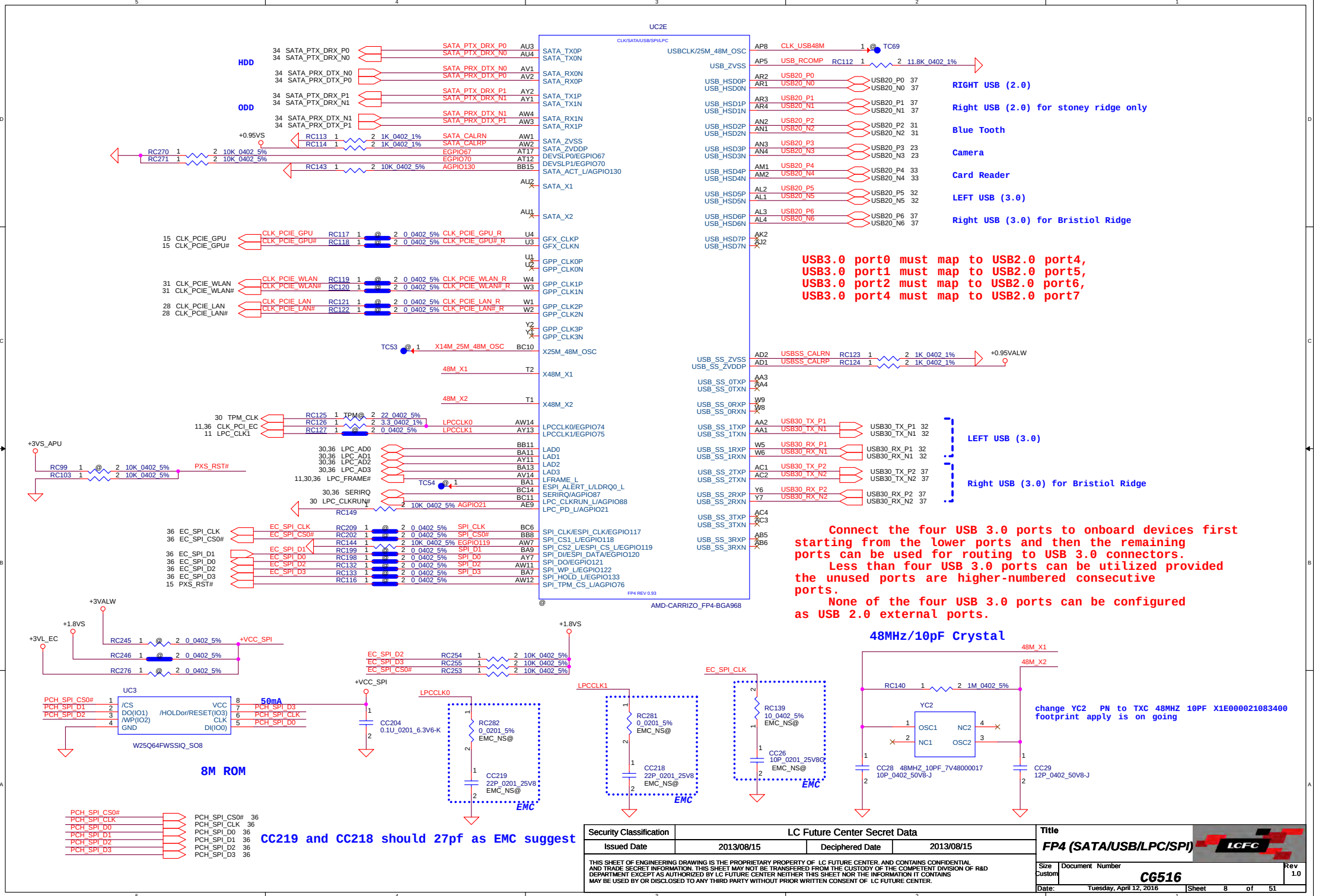
Date: Tuesday, April 12, 2016 | Sheet 7 of 51



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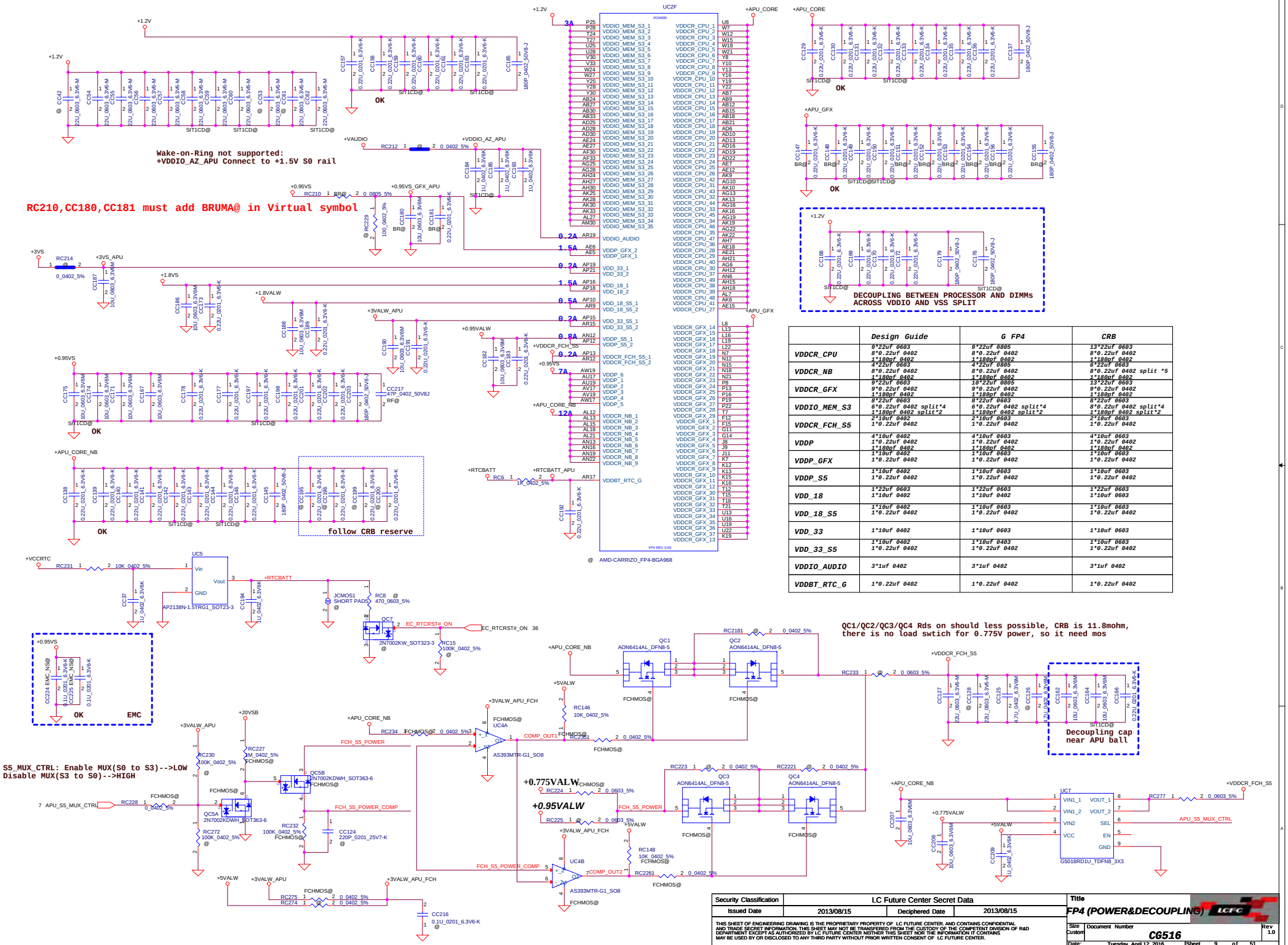

	Design Guide	G FP4	CRB
VDDCR_CPU	9*22uf 0603 8*0.22uf 0402 1*180pf 0402	9*22uf 0805 8*0.22uf 0402 1*180pf 0402	13*22uf 0603 8*0.22uf 0402 1*180pf 0402
VDDCR_NB	4*22uf 0603 8*0.22uf 0402 1*180pf 0402	4*22uf 0805 8*0.22uf 0402 1*180pf 0402	6*22uf 0603 8*0.22uf 0402 split *5 1*180pf 0402
VDDCR_GFX	9*22uf 0603 9*0.22uf 0402 1*180pf 0402	10*22uf 0805 9*0.22uf 0402 1*180pf 0402	13*22uf 0603 9*0.22uf 0402 1*180pf 0402
VDDIO_MEM_S3	8*22uf 0603 6*0.22uf 0402 split*4 1*180pf 0402 split*2	8*22uf 0603 6*0.22uf 0402 split*4 1*180pf 0402 split*2	8*22uf 0603 8*0.22uf 0402 split*4 1*180pf 0402 split*2
VDDCR_FCH_S5	2*10uf 0402 1*0.22uf 0402	2*10uf 0603 1*0.22uf 0402	2*10uf 0603 1*0.22uf 0402
VDDP	4*10uf 0402 1*0.22uf 0402 1*180pf 0402	4*10uf 0603 1*0.22uf 0402 1*180pf 0402	4*10uf 0603 1*0.22uf 0402 1*180pf 0402
VDDP_GFX	1*10uf 0402 1*0.22uf 0402	1*10uf 0603 1*0.22uf 0402	1*10uf 0603 1*0.22uf 0402
VDDP_S5	1*10uf 0402 1*0.22uf 0402	1*10uf 0603 1*0.22uf 0402	1*10uf 0603 1*0.22uf 0402
VDD_18	1*22uf 0603 1*10uf 0402	1*22uf 0603 1*10uf 0402	1*22uf 0603 1*10uf 0603
VDD_18_S5	1*10uf 0402 1*0.22uf 0402	1*10uf 0603 1*0.22uf 0402	1*10uf 0603 1*0.22uf 0402
VDD_33	1*10uf 0402	1*10uf 0603	1*10uf 0603
VDD_33_S5	1*10uf 0402 1*0.22uf 0402	1*10uf 0403 1*0.22uf 0402	1*10uf 0603 1*0.22uf 0402
VDDIO_AUDIO	3*1uf 0402	3*1uf 0402	3*1uf 0402
VDDBT_RTC_G	1*0.22uf 0402	1*0.22uf 0402	1*0.22uf 0402

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Title: FP4 (POWER&DECOUPLING)

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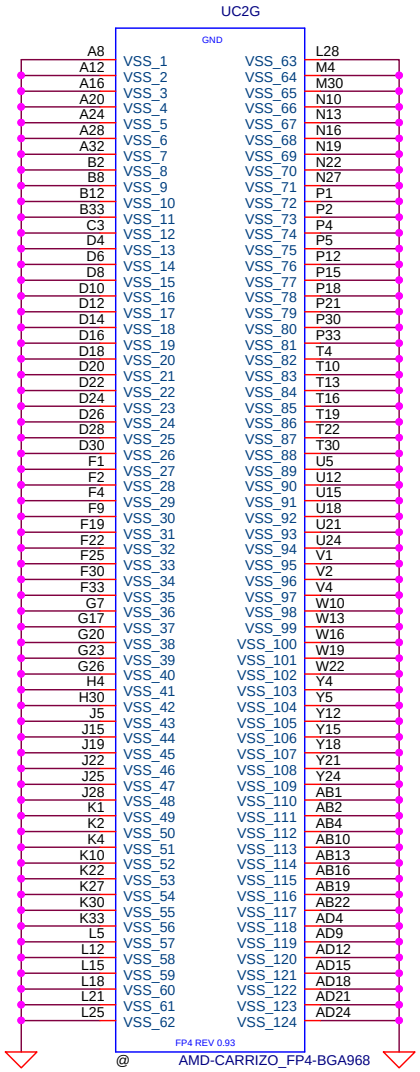
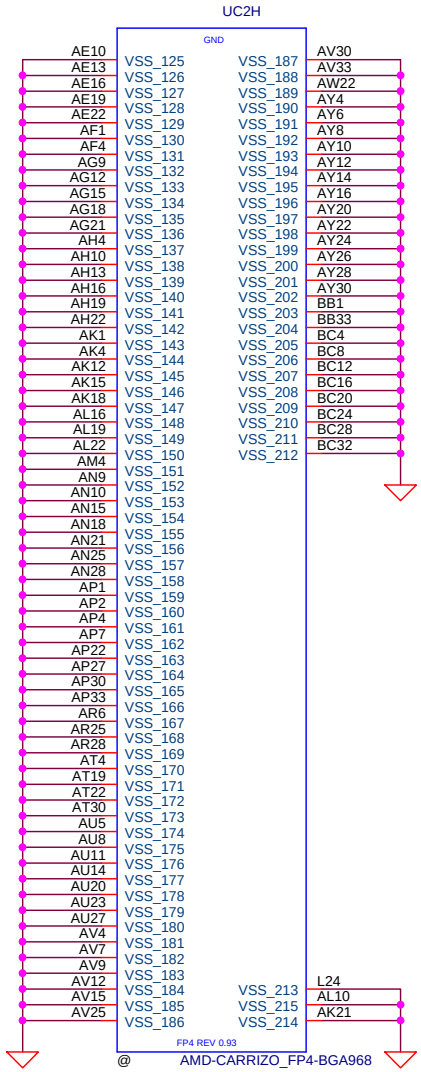
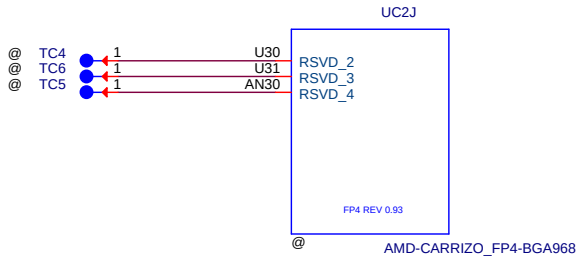
Date: Tuesday, April 12, 2016 | Sheet 9 of 51







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Title
FP4 (VSS)

Size	Document Number	Rev
Custom	CG516	1.0

Date: Tuesday, April 12, 2016 Sheet 10 of 51

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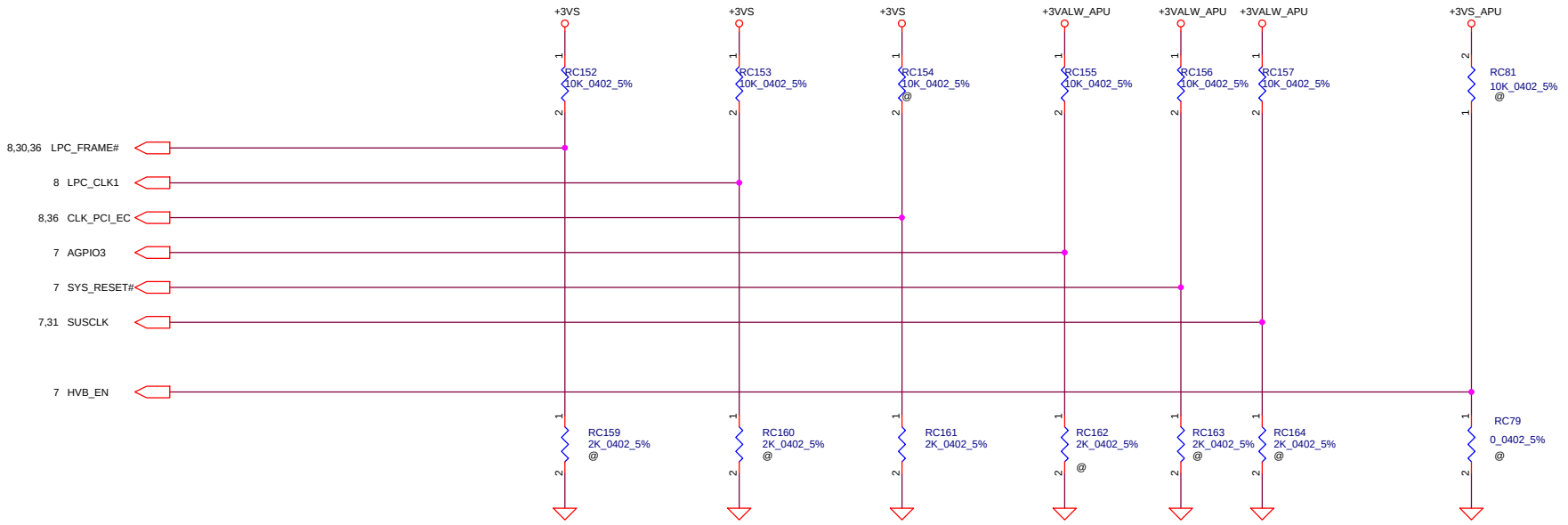

STRAP PINS

Signal	LFRAME_L	LPCCLK1	LPCCLK0	RTCCLK Int pull-up	SYS_RESET_L Int pull-up	AGPIO3 Int pull-up	HVB_EN
Type	II	II	II	I	I	I	
PULL HIGH	SPI ROM Default	Internal CLK Gen Default	Boot Fail Timer Enabled	RTC Coin Battery is implemented Default	Normal Power Up &Reset Timing Default	Enhanced reset logic (for quicker S5 resume) Default	floating Disable HVB on FP4 platforms Default
PULL LOW	LPC ROM	Reserved	Boot Fail Timer Disabled Default	RTC Coin Battery is not implemented	Reserved	traditional reset logic	connected to VSS Enable HVB on FP4 platforms

Type I straps become valid immediately after capture with the rising edge of RSMRST_L,they are captured only once when power is first applied to the processor

Type II straps become valid after PWR_GOOD is asserted,straps are captured every time the systems powers up from the S5 state. A transition from S3 to S0 does not trigger capture.
Type II straps should be pulled up to S0 power rail to prevent leakage when the signal is connected to a device in S0 power domain.

If the LPC bus is connected to devices that are on S0 power rail, then a pull-up resistor to VDD_33 is implemented.

All Strap pins must be configured with either external pull-up or pull-down resistors.

Platforms that are designed for AOAC complaint are recommended to use the Alternate Reset by strapping this pin to ' 1' for AGPIO3

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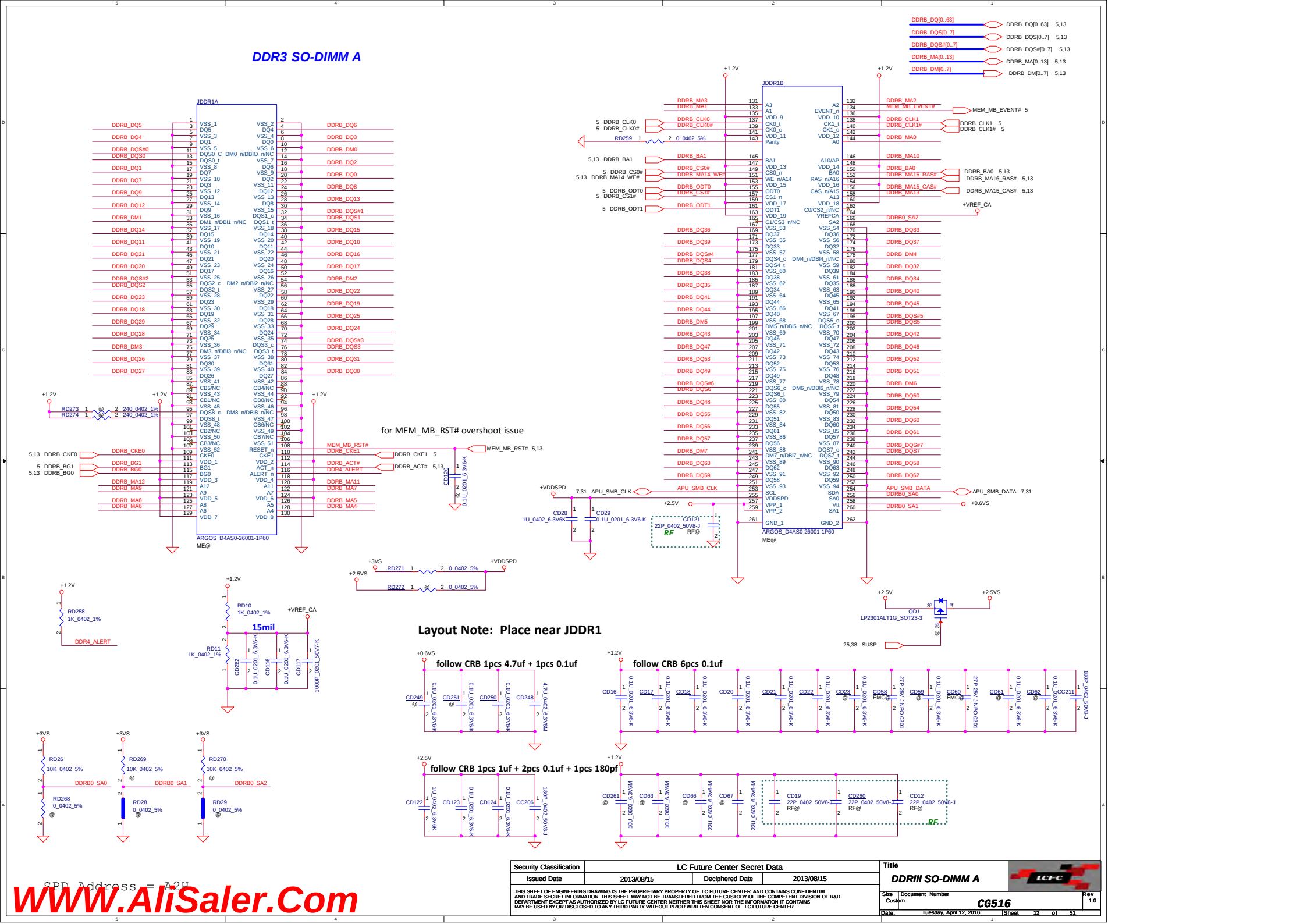
Date: Tuesday, April 12, 2016 | Sheet 11 of 51

DDR3 SO-DIMM A



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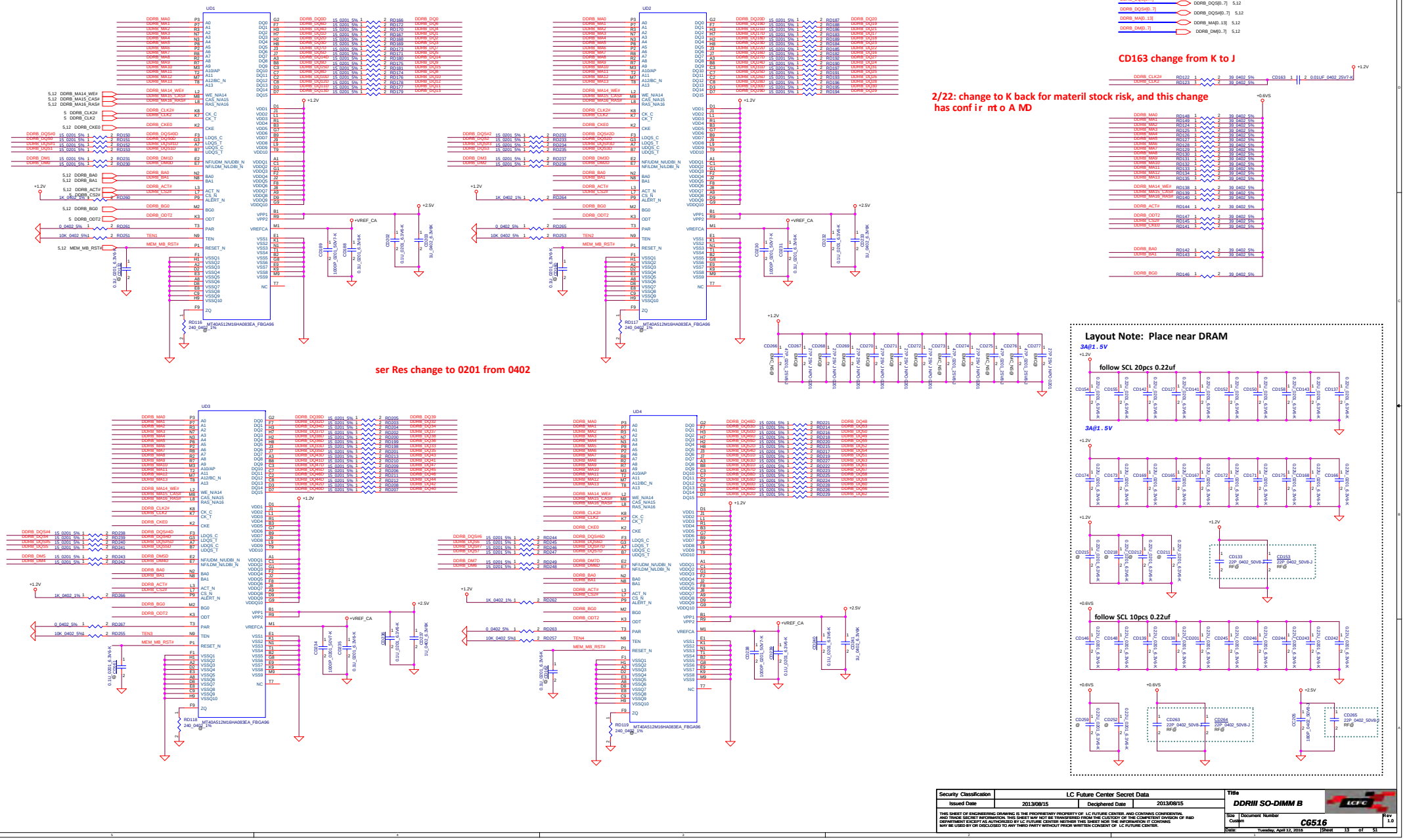

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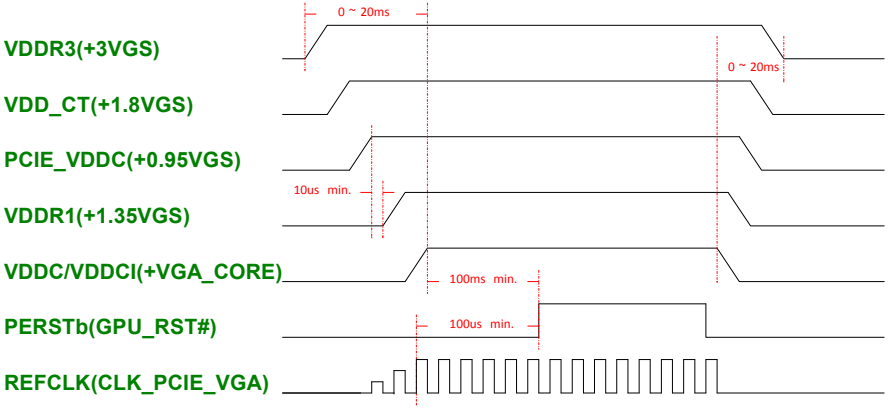
Size: Custom | Document Number: CG516 | Rev: 1.0

Date: Tuesday, April 12, 2016 | Sheet 13 of 51

Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µ s.
It is recommended that the 3.3-V rail ramp up first.
The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 µ s before VDDC, VDDCI, and VMEMIO start to ramp up.
The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/µ s).
For power down, reversing the ramp-up sequence is recommended.



VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
128Mx16	NA	100	4.53K	4.99K
	NA	111	4.75K	NC
	NA	110	3.4K	10K
256Mx16	Hynix H5TC4G63CFR-N0C 4Gb 900(1G)	000	NC	4.75K
	Micron MT41J256M16LY-091G:N 4Gb 900(1G)	010	4.53K	2K
	Samsung K4W4G1646E-BC1A 4Gb 900(1G)	001	8.45K	2K

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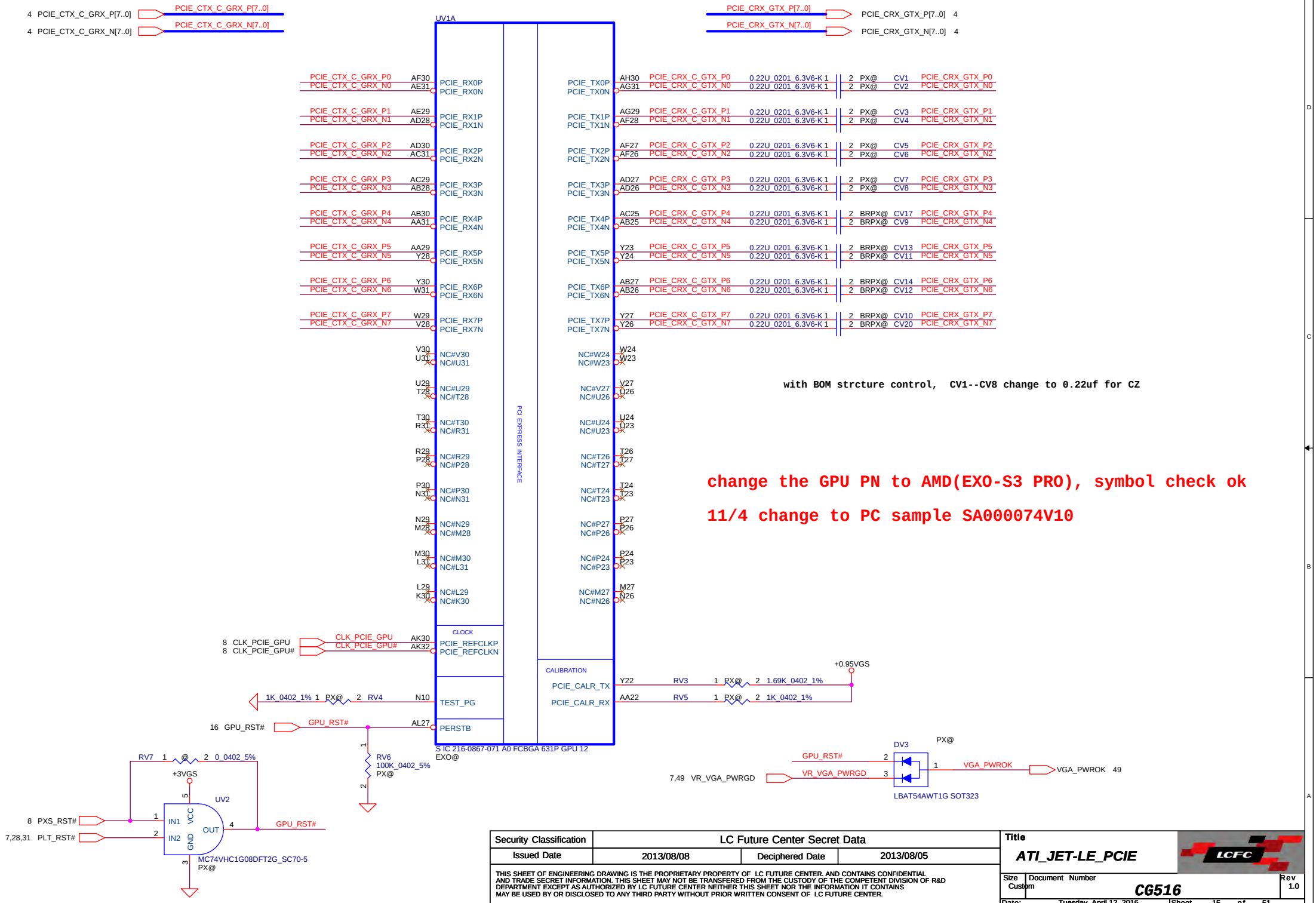

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Title: ATI_JET-LE_PCIE

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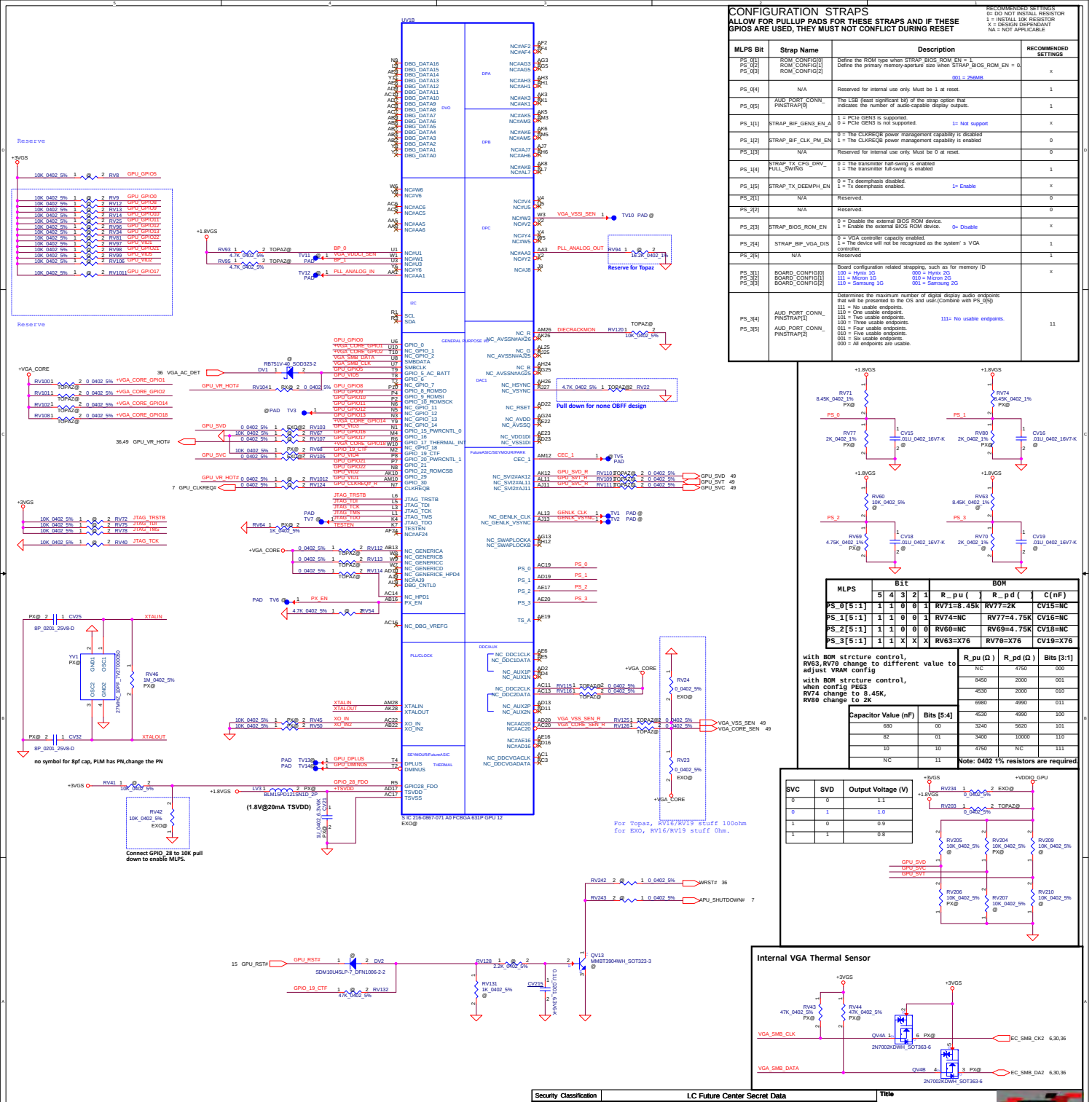
Date: Tuesday, April 12, 2016 | Sheet 15 of 51



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	Define the ROM type when STRAP_BIOS_ROM_EN = 1. Define the primary memory-aperture size when STRAP_BIOS_ROM_EN = 0. 001 = 256MB	x
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported. 1= Not support	x
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled. 1= Enable	x
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device. 0= Disable	x
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system' s VGA controller.	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID 100 = Hynix 1G 000 = Hynix 2G 111 = Micron 1G 010 = Micron 2G 110 = Samsung 1G 001 = Samsung 2G	x
PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user.(Combine with PS_0[5]) 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 111= No usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	11

MLPS	Bit					BOM		
	5	4	3	2	1	R_pu ( )	R_pd ( )	C(nF)
PS_0[5:1]	1	1	0	0	1	RV71=8.45k	RV77=2K	CV15=NC
PS_1[5:1]	1	1	0	0	1	RV74=NC	RV77=4.75K	CV16=NC
PS_2[5:1]	1	1	0	0	0	RV60=NC	RV69=4.75K	CV18=NC
PS_3[5:1]	1	1	X	X	X	RV63=X76	RV70=X76	CV19=X76

with BOM strcture control, RV63,RV70 change to different value to adjust VRAM config

with BOM strcture control, when config PE63 RV74 change to 8.45K, RV80 change to 2K

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required

SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Internal VGA Thermal Sensor

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Title: ATI_JET-LE_Main_MSIC

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Date: Tuesday, April 12, 2016 | Sheet 16 of 51

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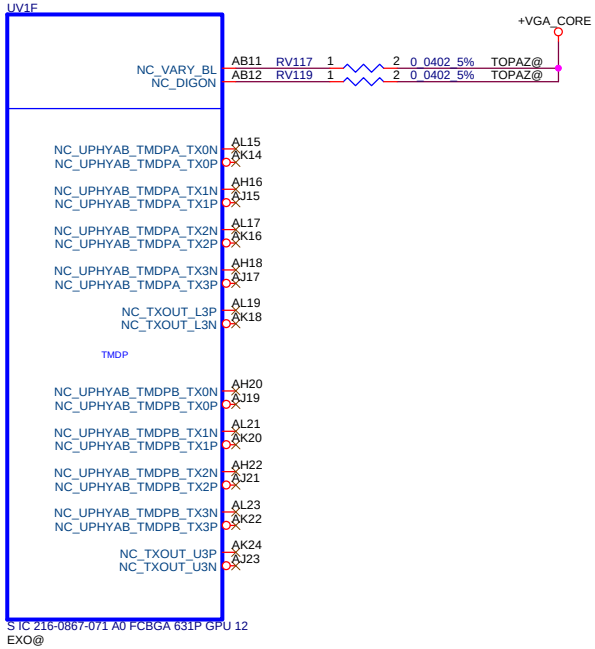

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Title
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Size	Document Number	Rev
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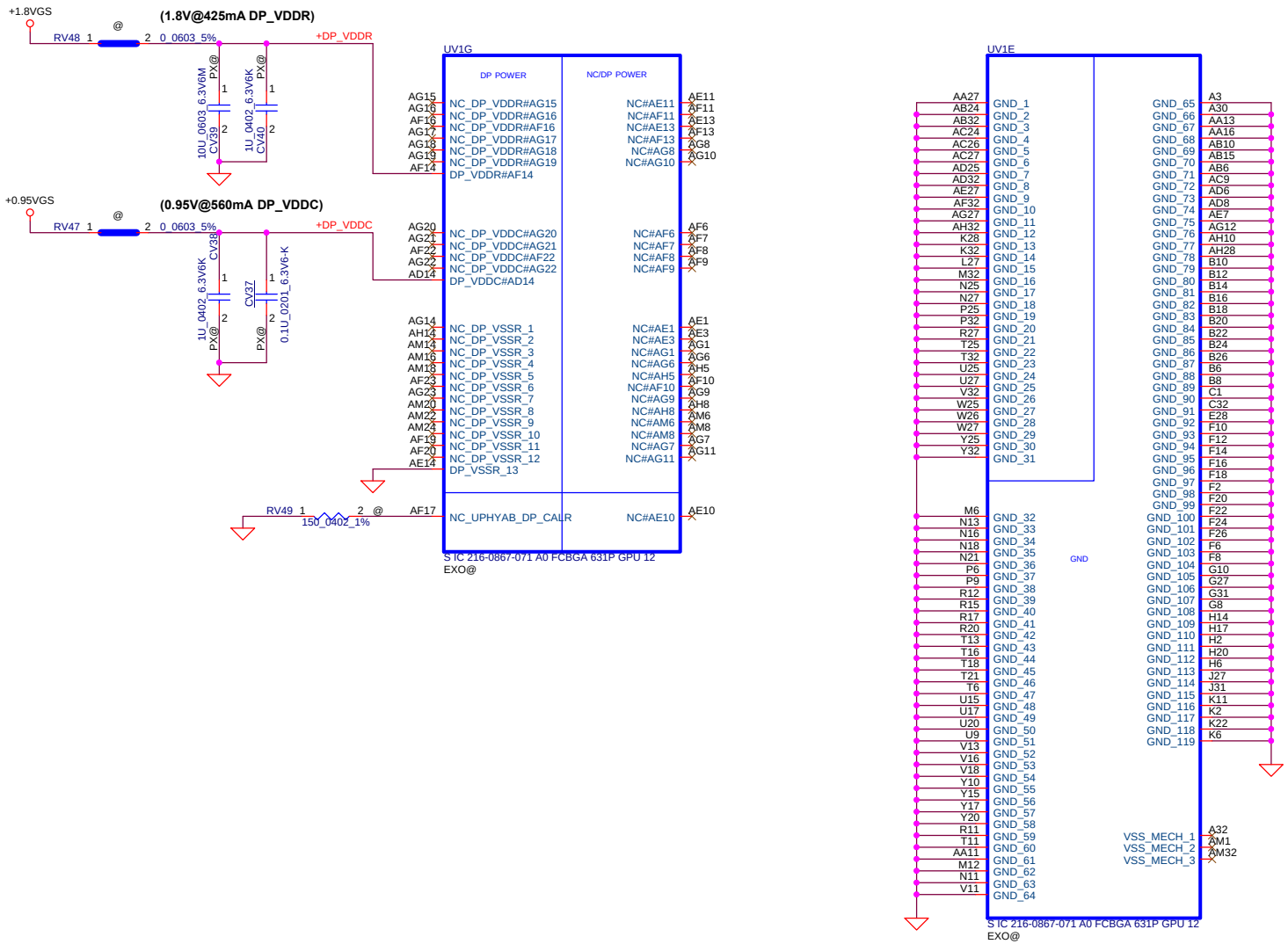
Date: Tuesday, April 12, 2016 Sheet 17 of 51



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Title

ATI_JET-LE_DP Power

LCFC

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Custom	CG516	1.0

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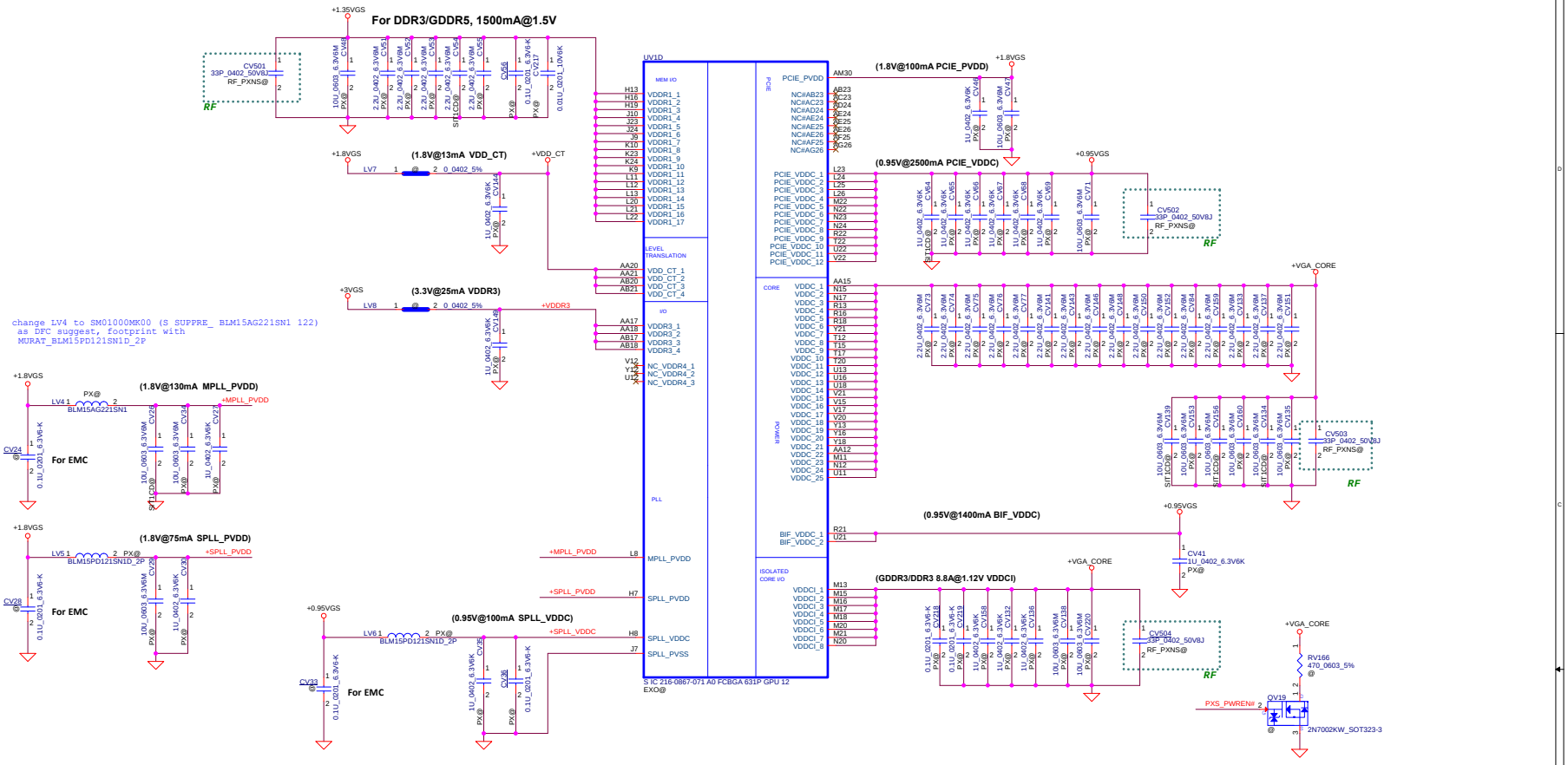
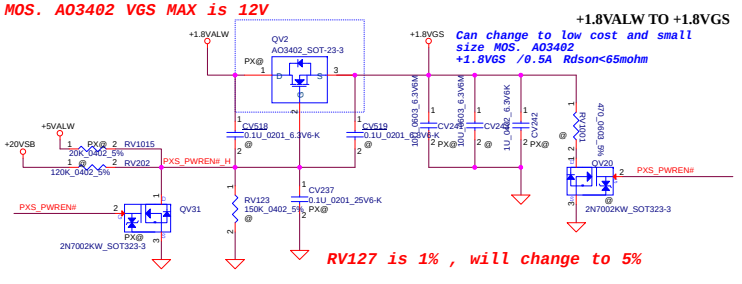
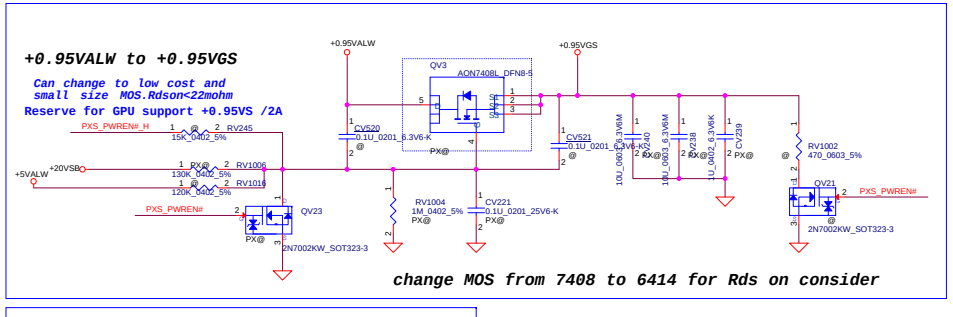
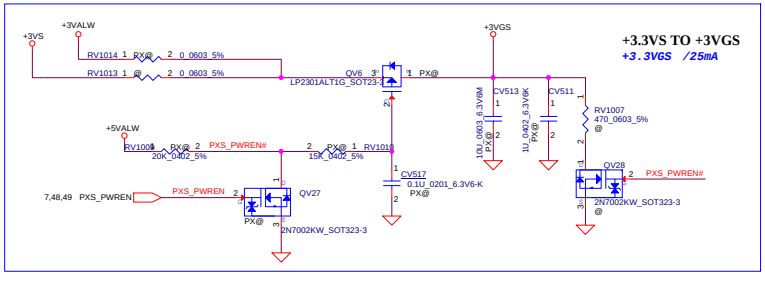
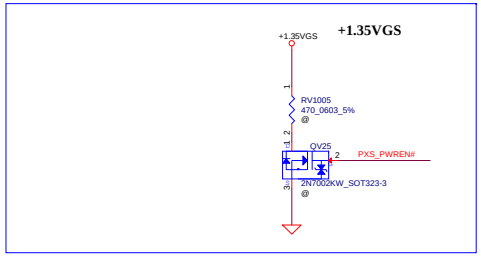


MOS. AO3402 VGS MAX is 12V









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Title: ATI_JET-LE_Power

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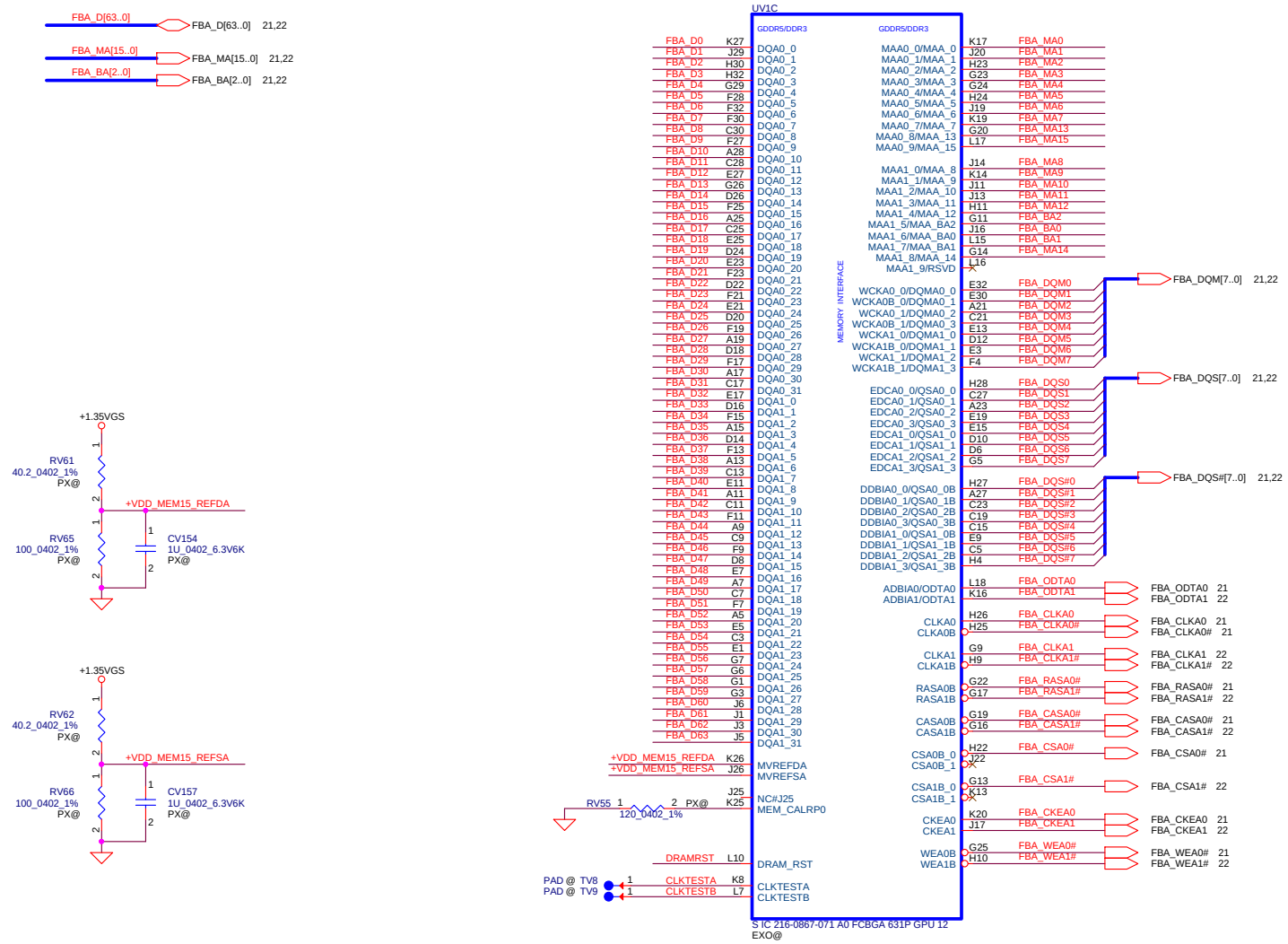

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Title
ATI_JET-LE_MEM IF

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Date: Tuesday, April 12, 2016 | Sheet 20 of 51

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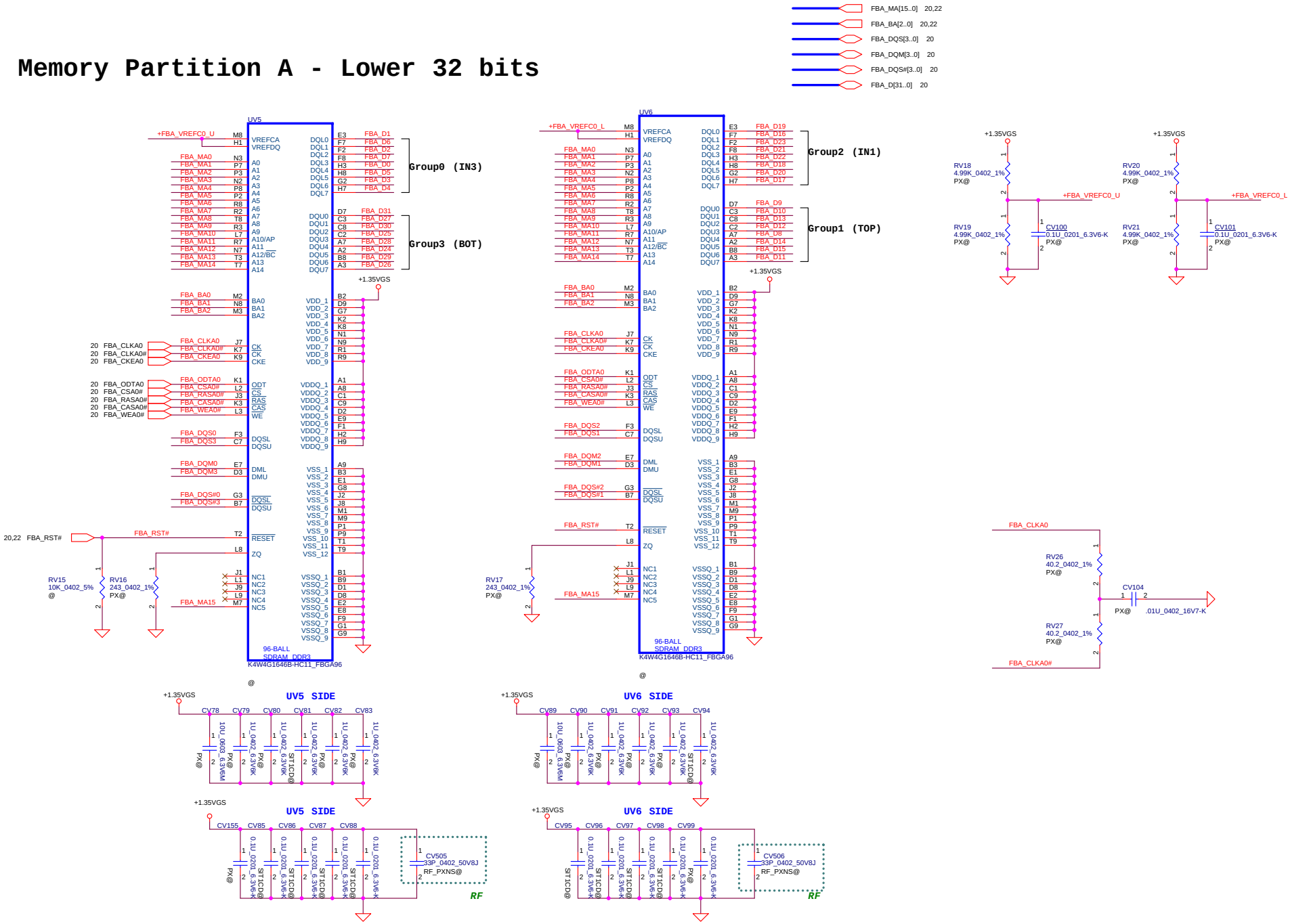
Memory Partition A - Lower 32 bits



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Title: ATI_JET-LE_VRAM_A

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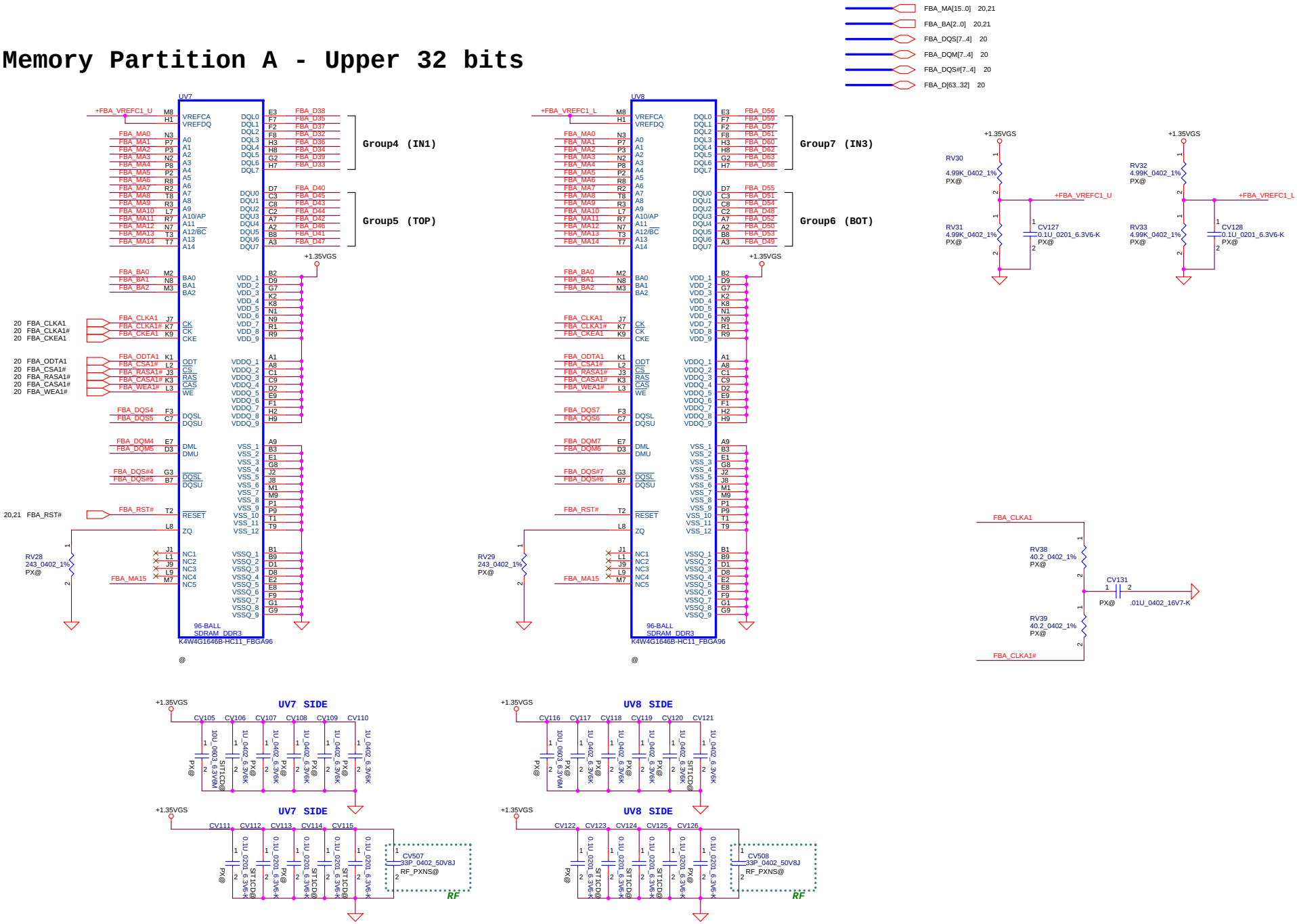
Date: Tuesday, April 12, 2016 | Sheet 21 of 51

Memory Partition A - Upper 32 bits



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Title: ATI_JET-LE_VRAM_B

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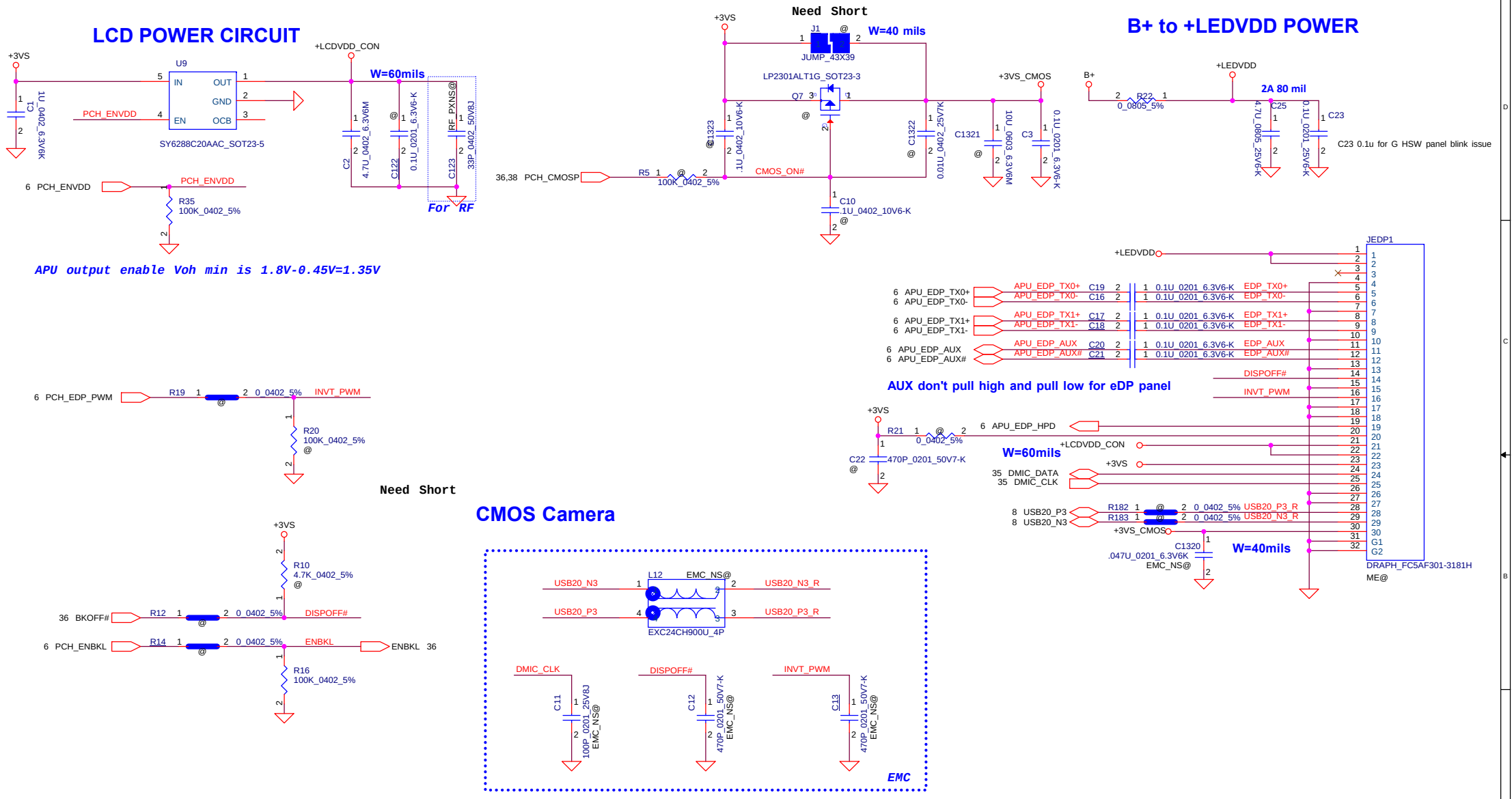

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Title: eDP/CMOS

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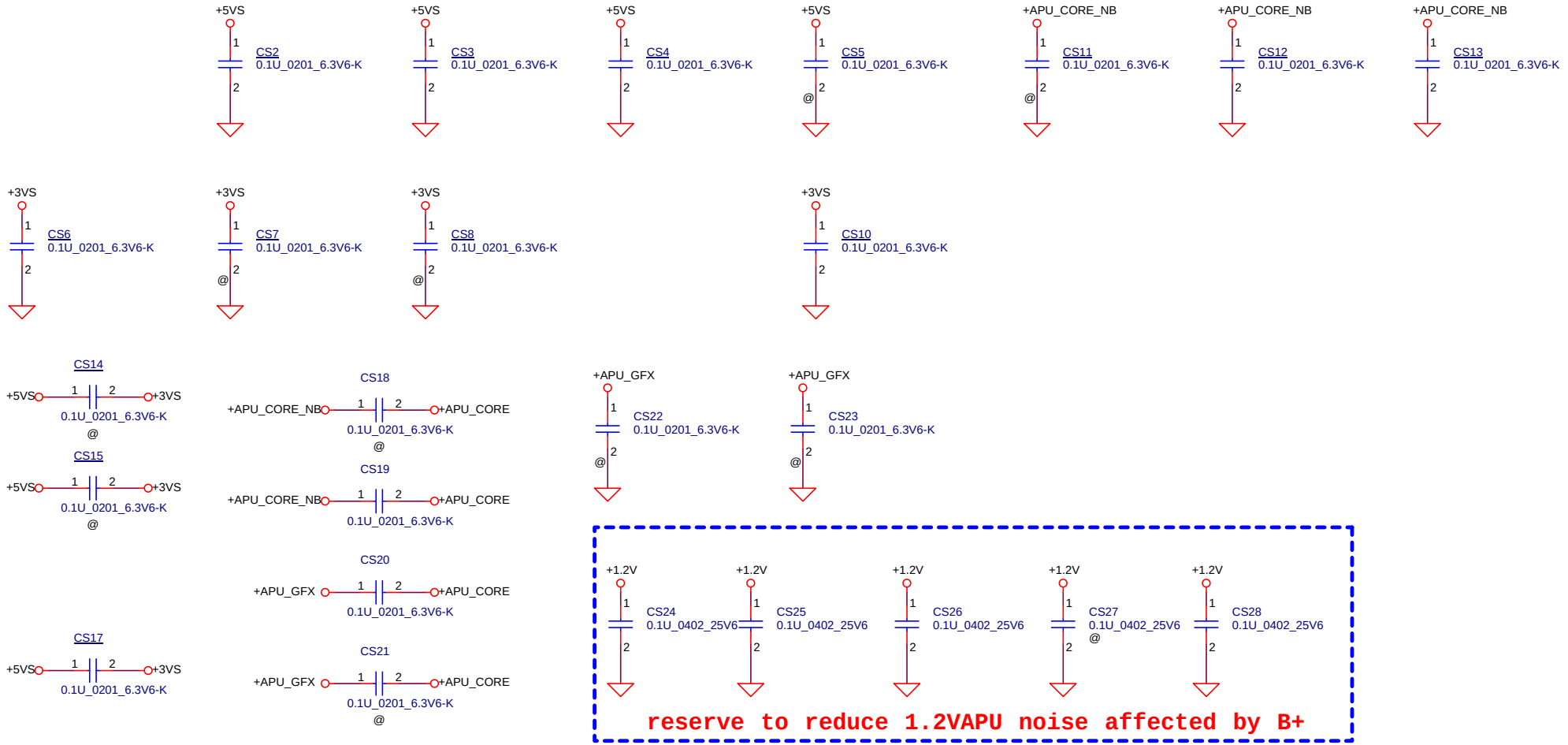
Date: Tuesday, April 12, 2016 | Sheet 23 of 51



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Title: StitchingCap

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Date: Tuesday, April 12, 2016 | Sheet 24 of 51

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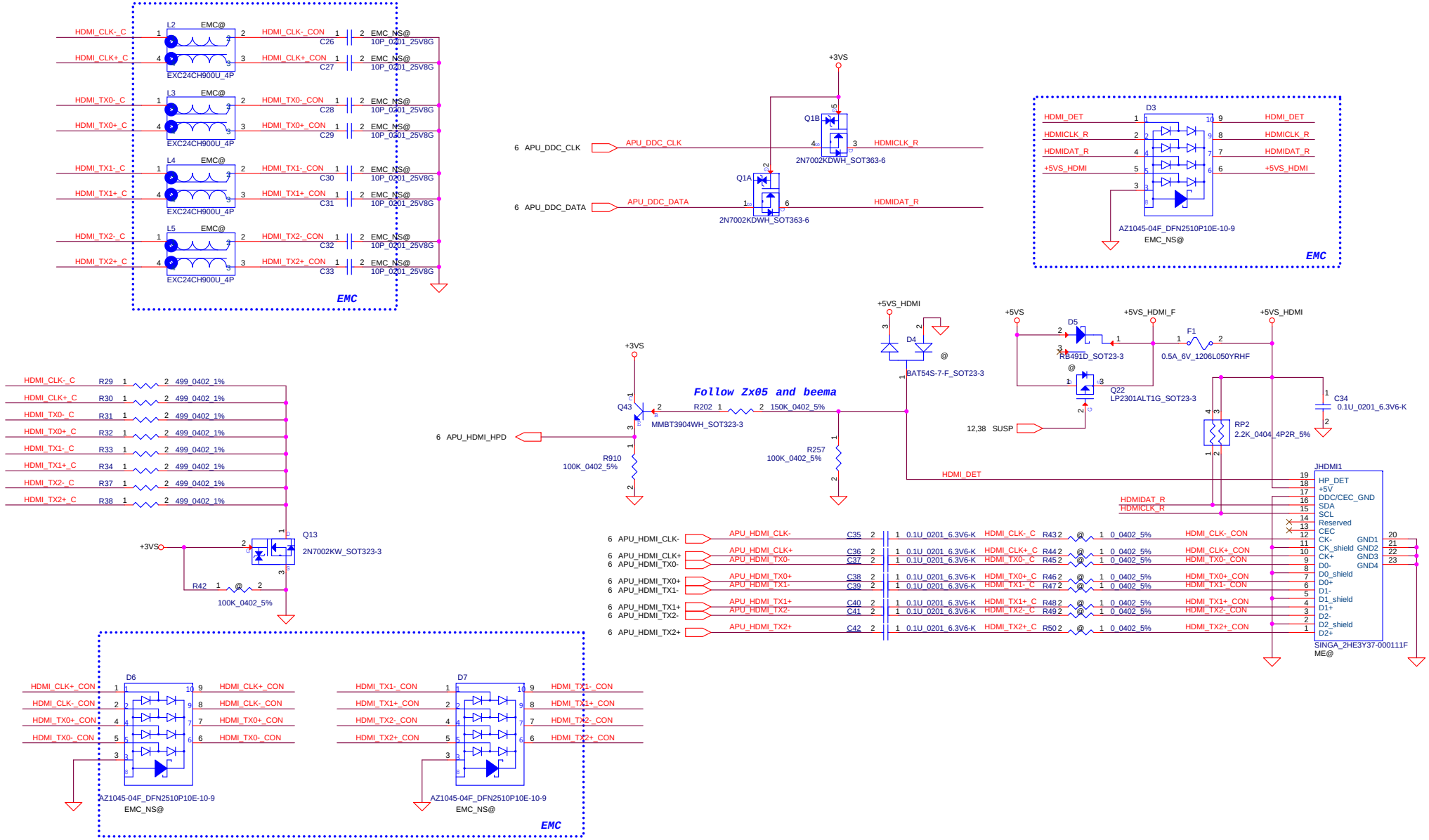

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Title: **HDMI_CONN**

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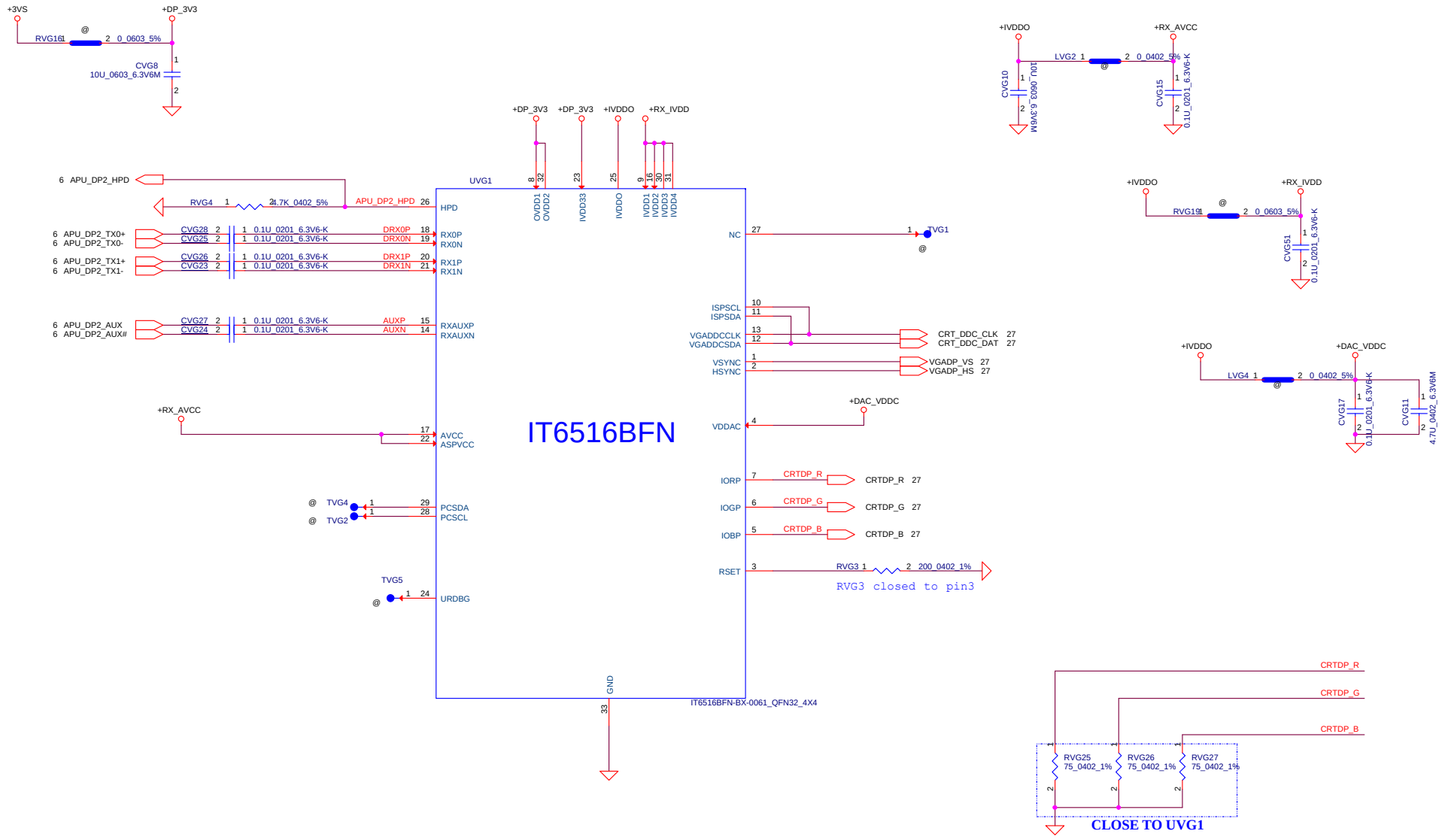

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Title: DP to CRT Convert(IT6515FN)

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Date: Tuesday, April 12, 2016 | Sheet 26 of 51

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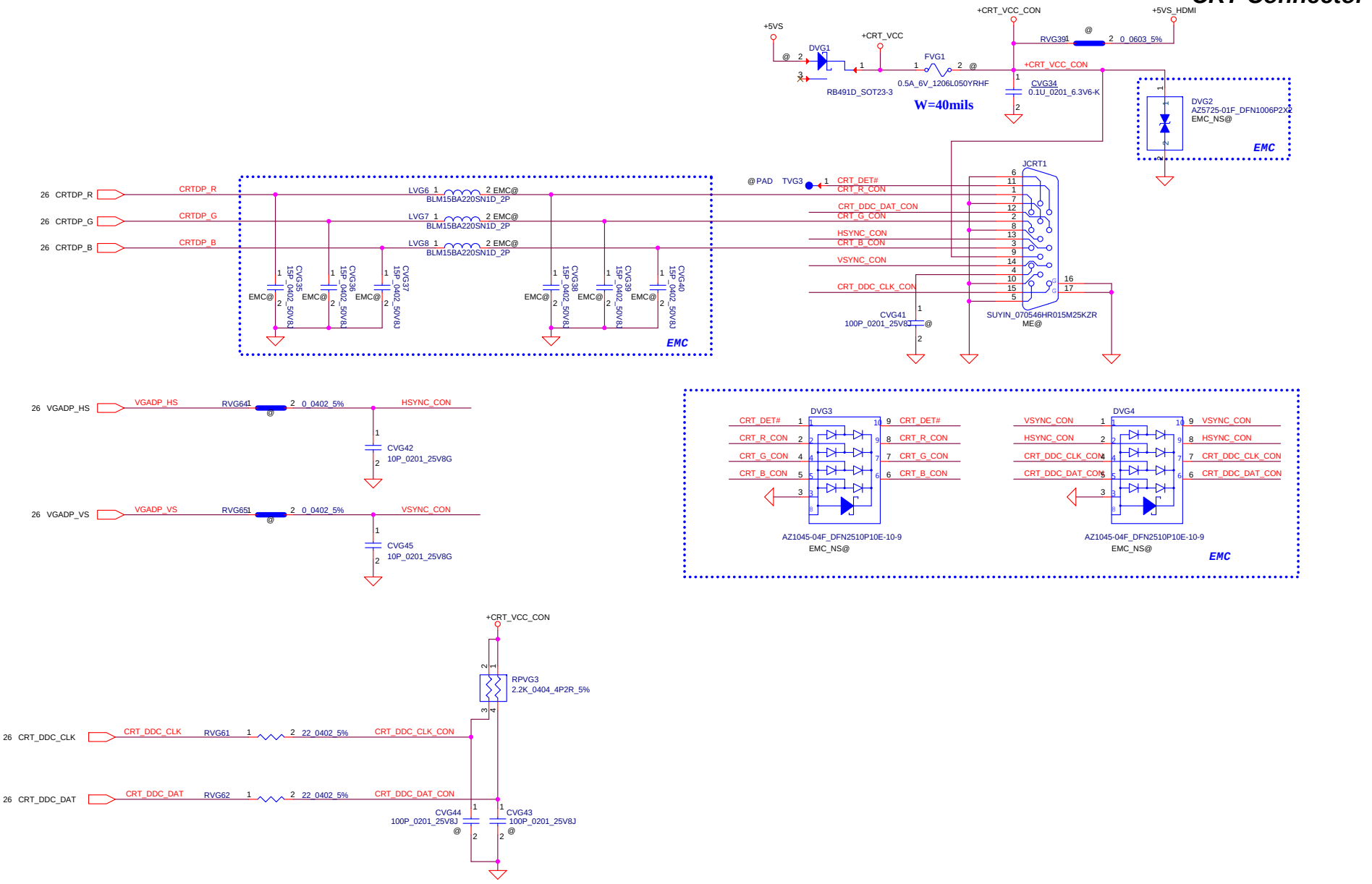
CRT Connector



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Title: CRT

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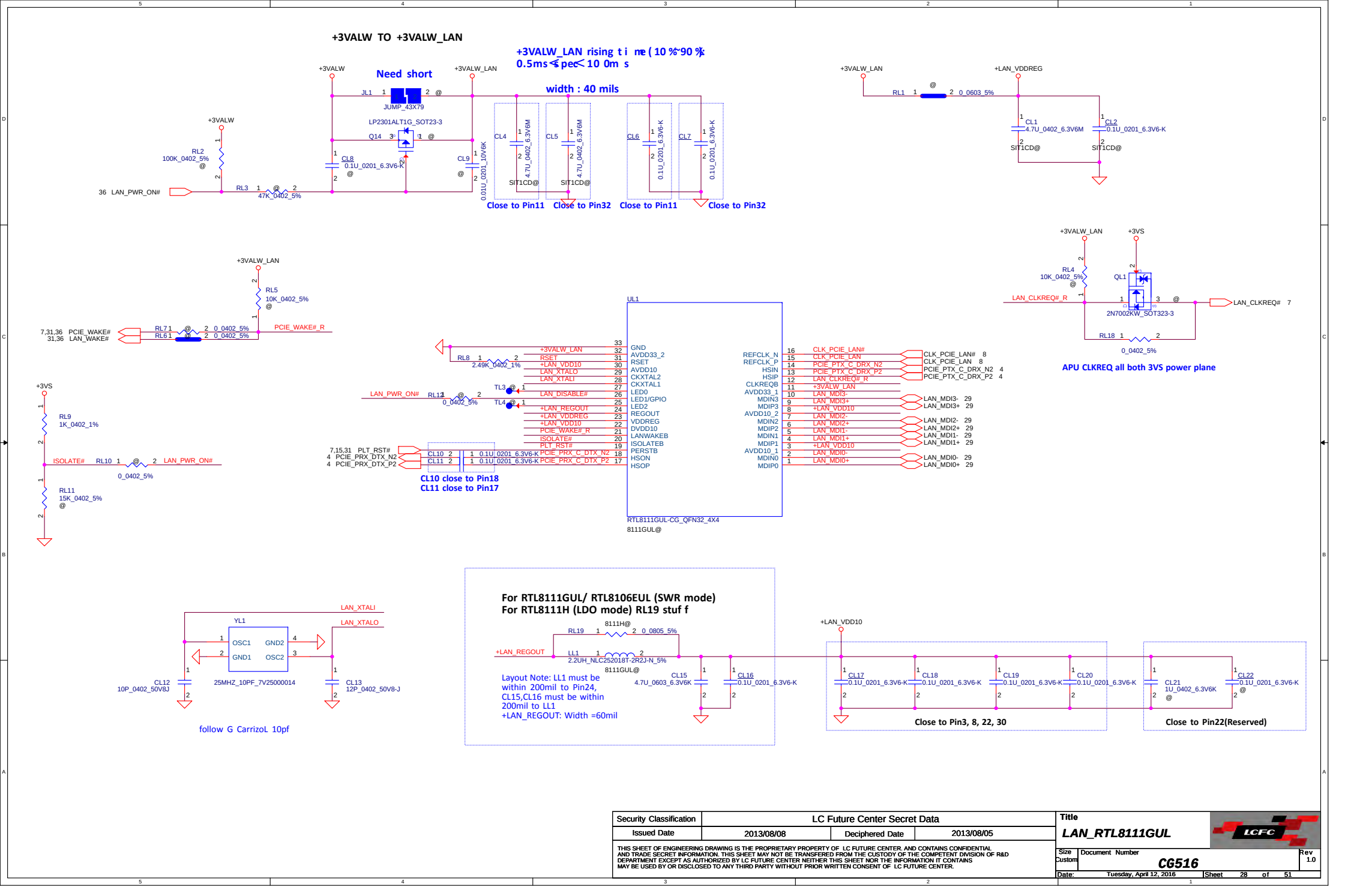

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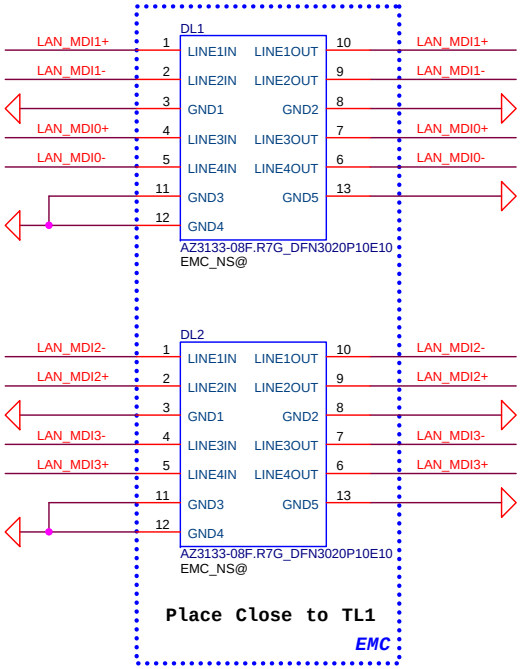
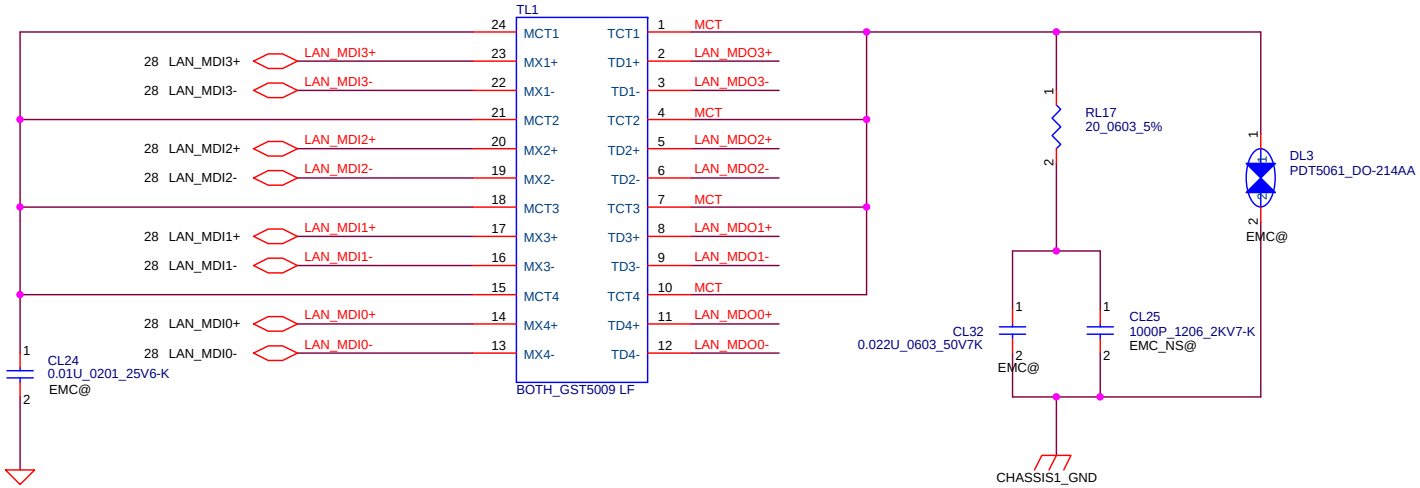
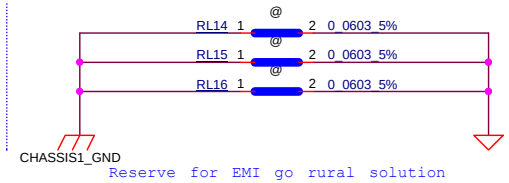
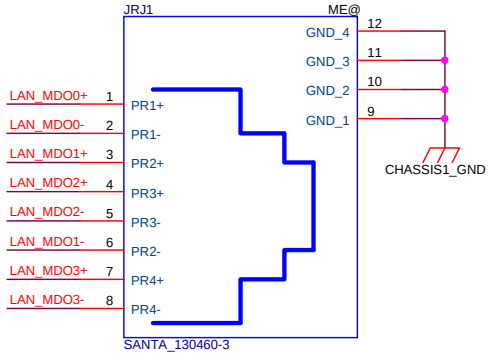
DL1/DL2
1'S PN:SC300003M00









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Issued Date	2013/08/08	Deciphered Date	2013/08/05

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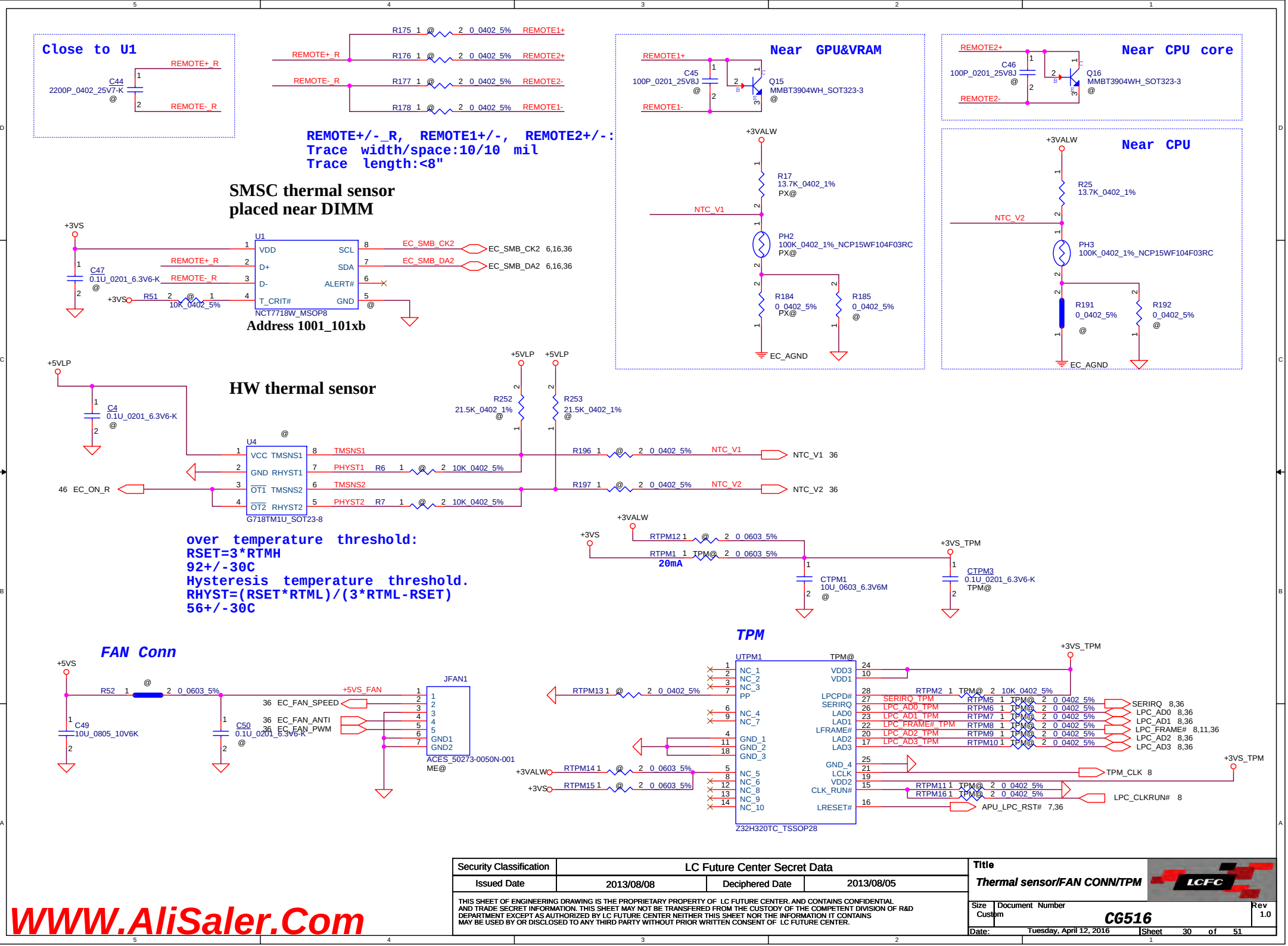
Title: LAN_Transformer

Size: B | Document Number: CG516 | Rev: 1.0

Date: Tuesday, April 12, 2016 | Sheet 29 of 51



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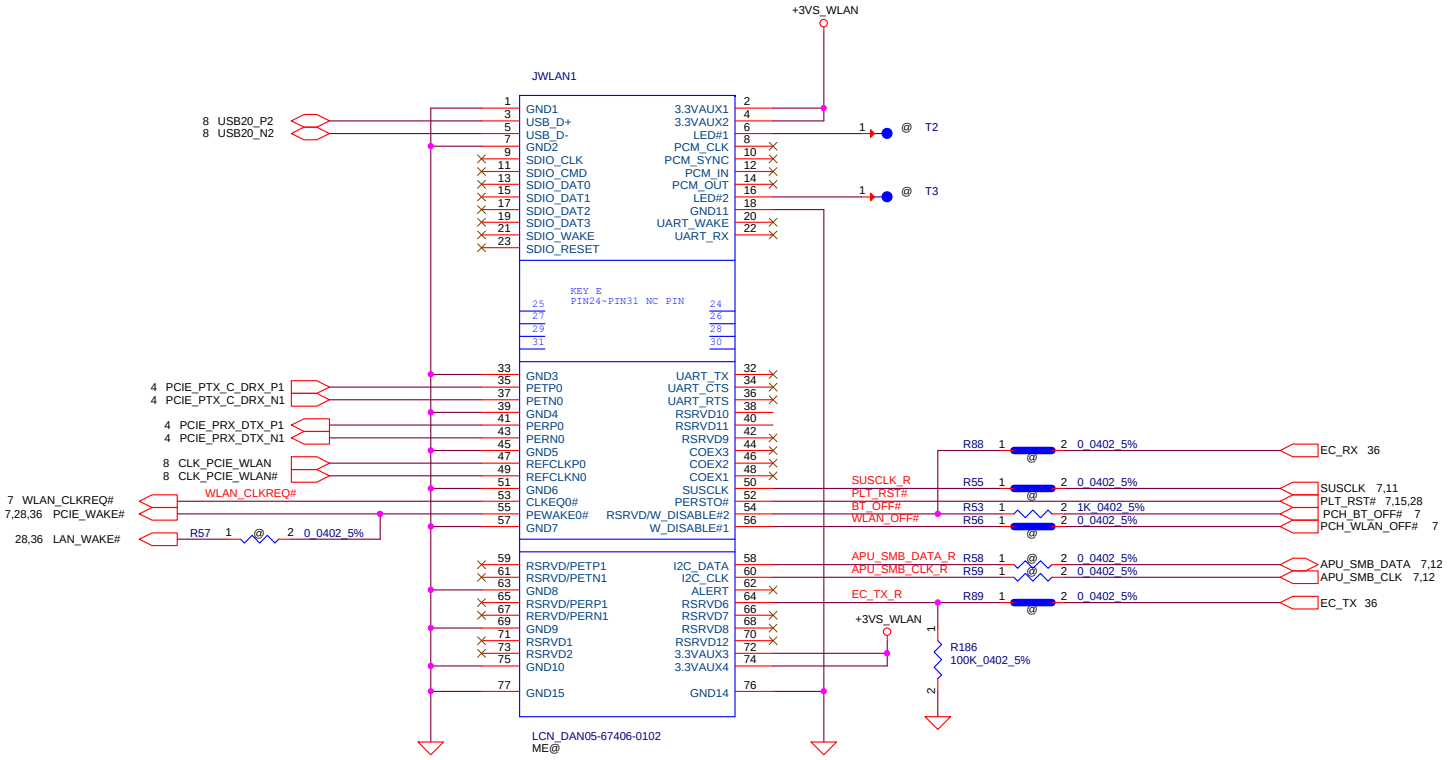
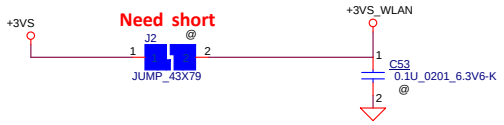
Mini-Express Card(WLAN/WiMAX)





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Title: NGFF WLAN

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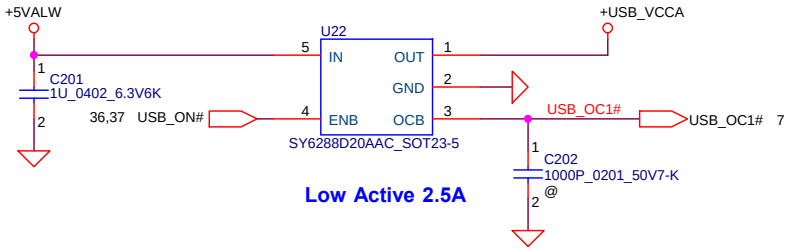
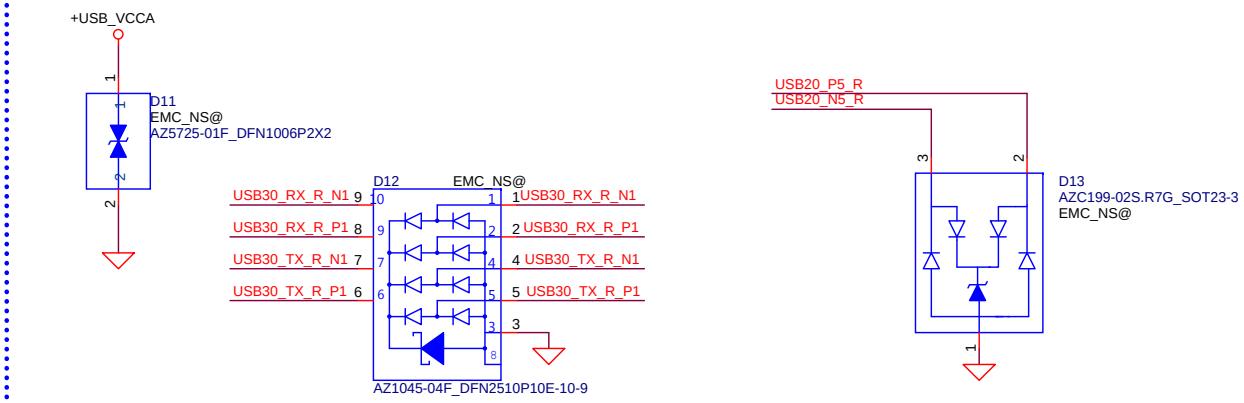
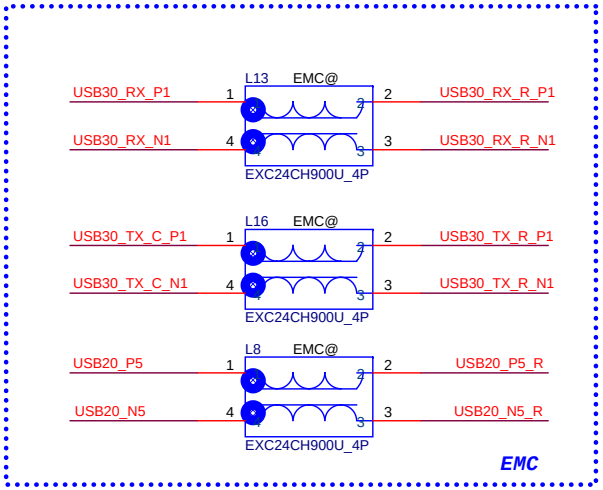
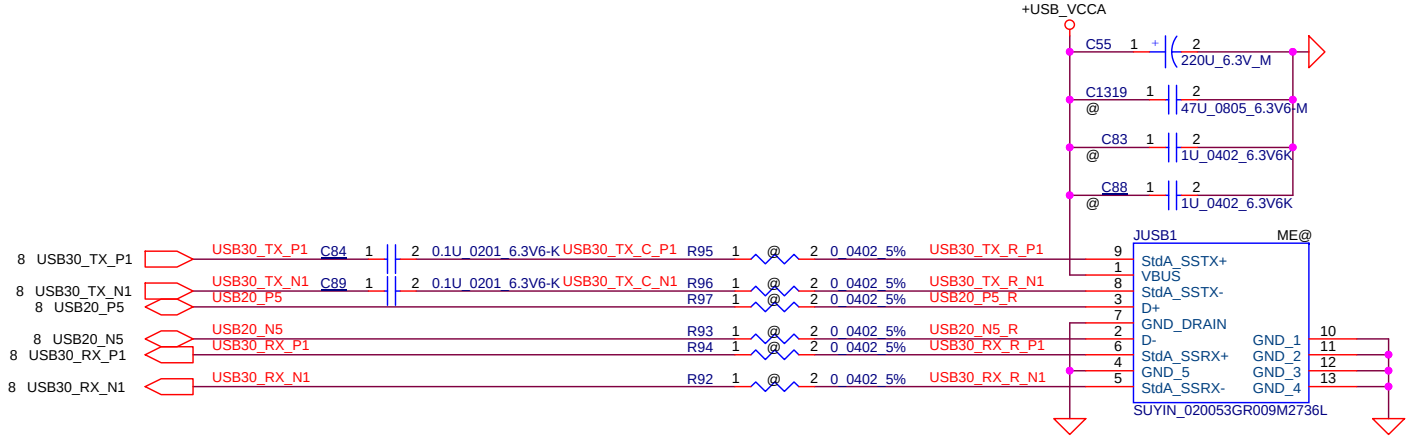
Date: Tuesday, April 12, 2016 | Sheet 31 of 51

Left Side USB3.0 Port X 1









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Issued Date	2013/08/08	Deciphered Date	2013/08/05

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Title: **USB PORT (LEFT)**

Size: Custom | Document Number: **CG516** | Rev: 1.0

Date: Tuesday, April 12, 2016 | Sheet 32 of 51

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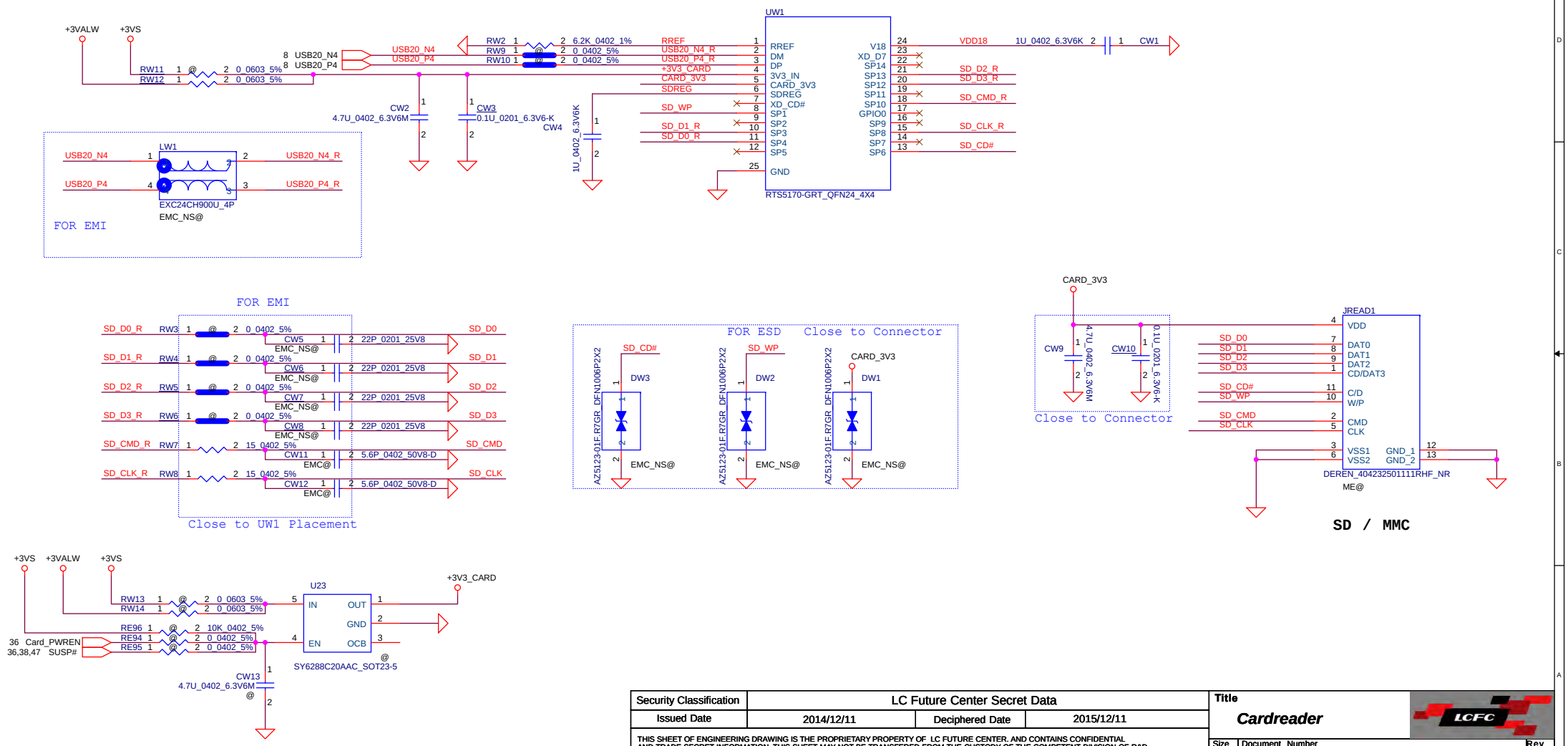

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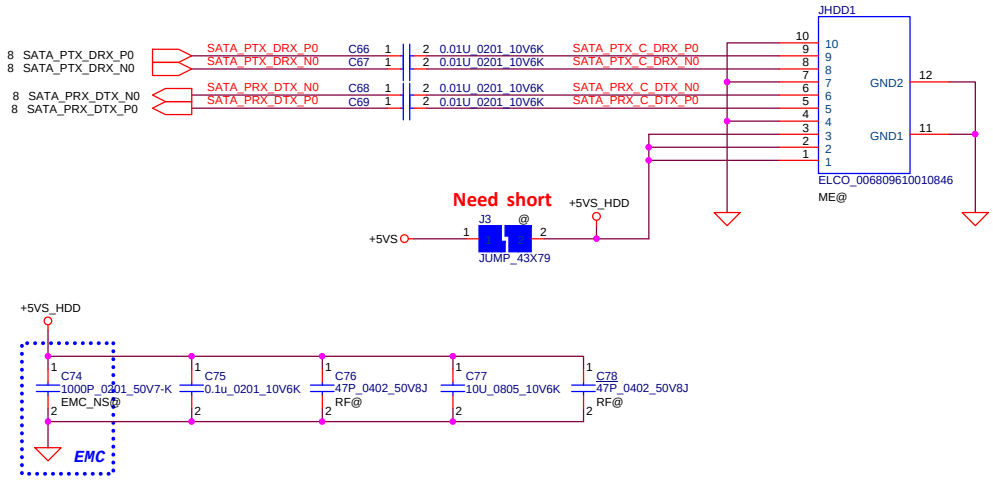
Title: **Cardreader**

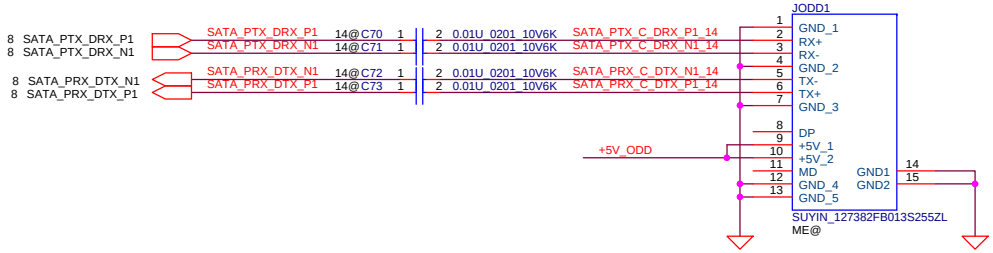
Size: Custom | Document Number: **CG516** | Rev: 1.0

Date: Tuesday, April 12, 2016 | Sheet 33 of 51

SATA HDD Conn.

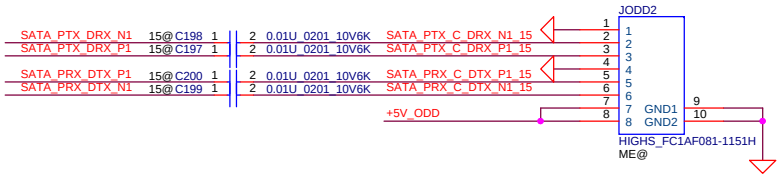


FOR 14" SATA ODD Conn.

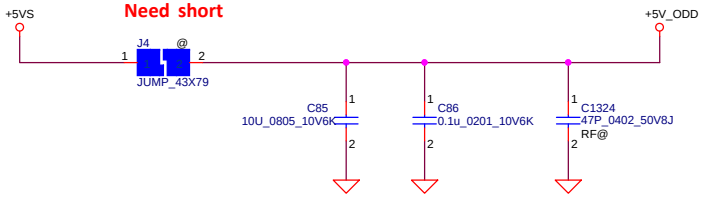


FOR 15" SATA ODD FFC Conn

SATA 15 ODD P/N pin assgin is different from G SKL



+5VS to +5V_ODD



ODD DA???

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Issued Date	2013/08/08	Deciphered Date	2013/08/05

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Title: **HDD/ODD CONN**

Size: Custom | Document Number: **CG516** | Rev: 1.0

Date: Tuesday, April 12, 2016 | Sheet 34 of 51

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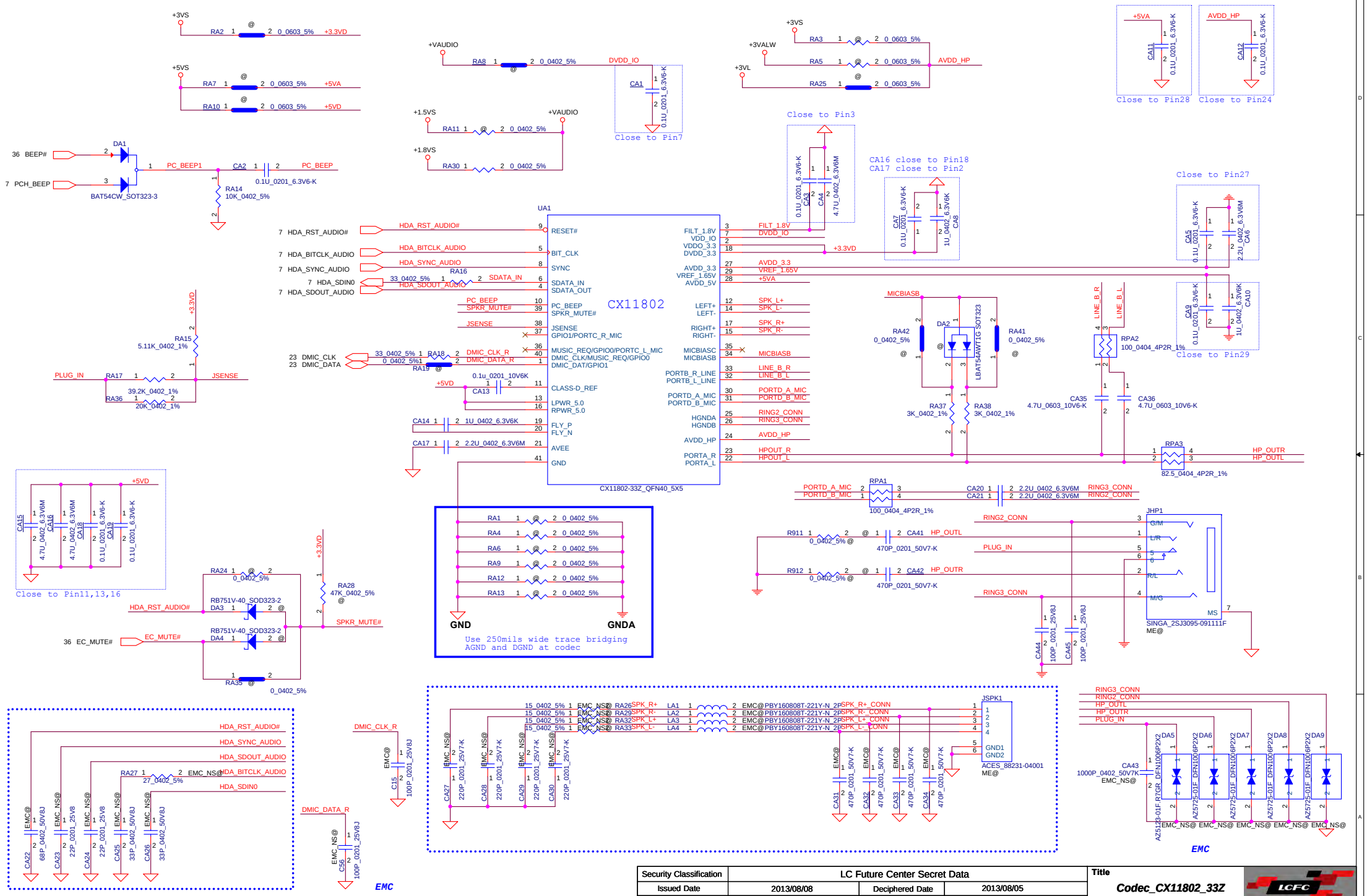

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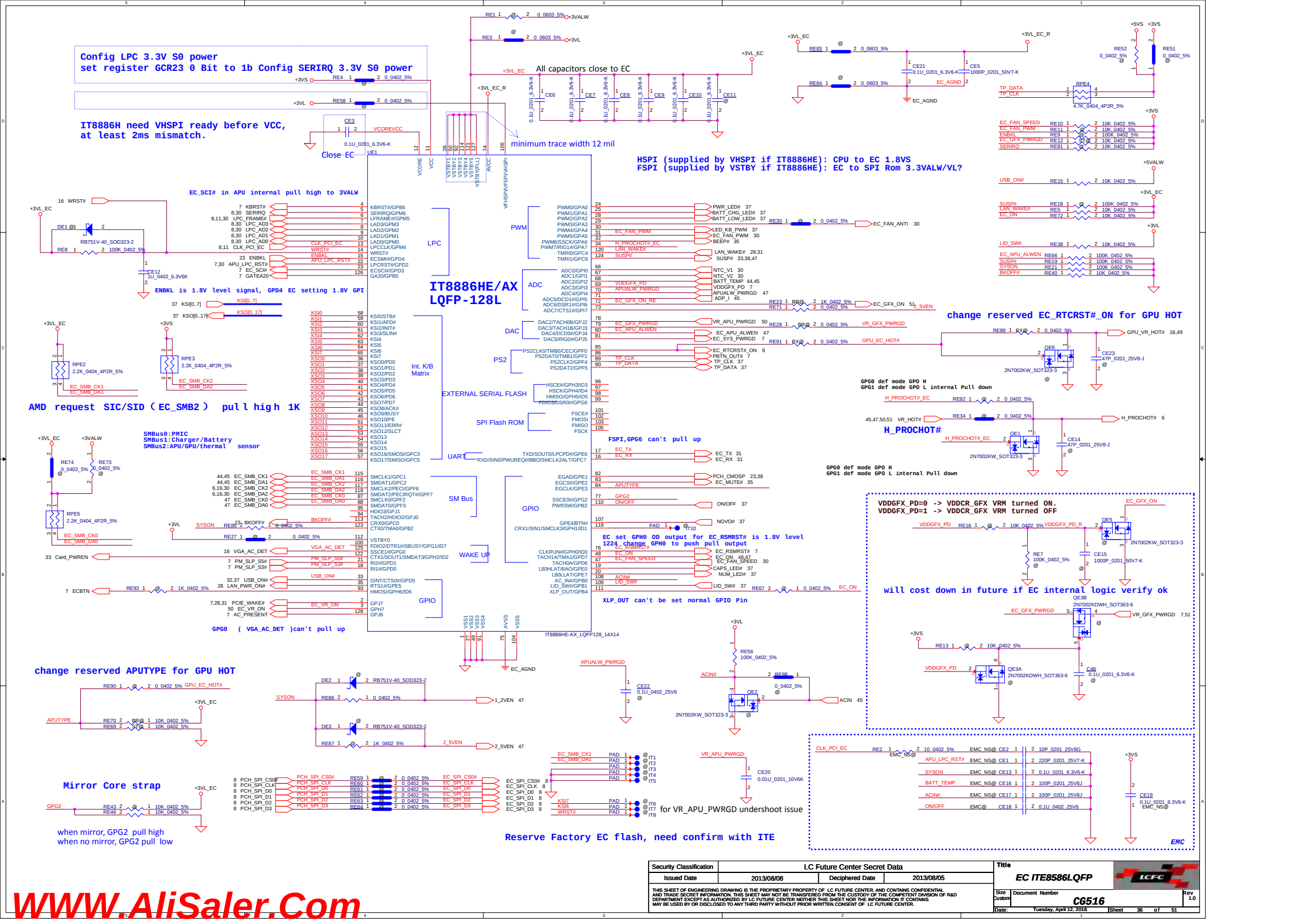

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Title: EC ITE8586LQFP

Size: Custom | Document Number: CG516 | Rev: 1.0

Date: Tuesday, April 12, 2016 | Sheet 36 of 51

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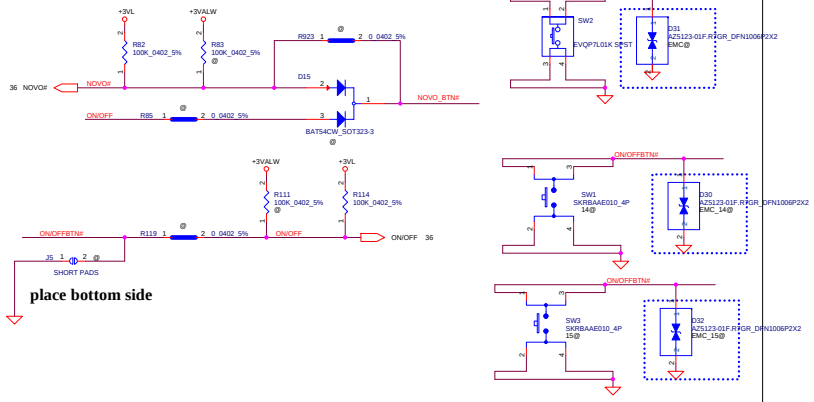
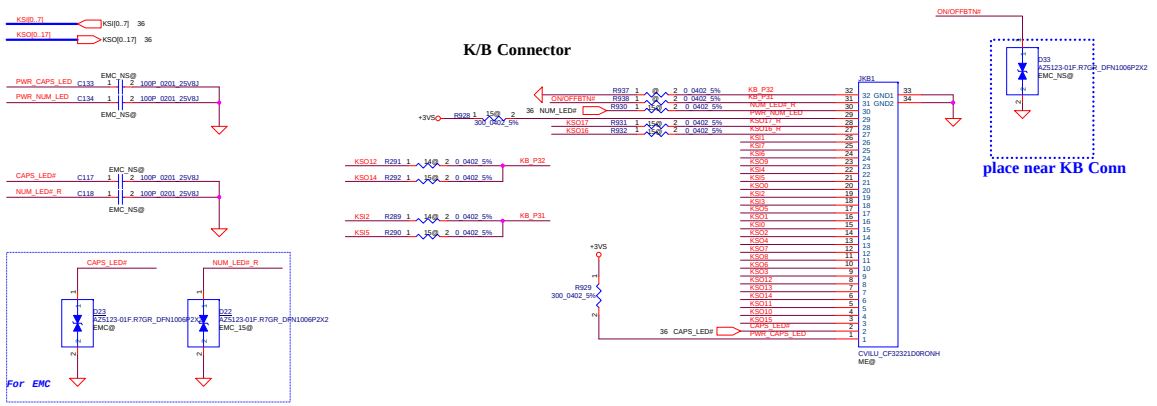
ON/OFF switch



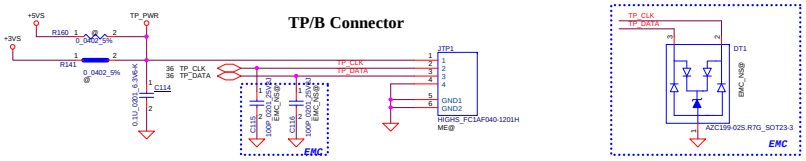
place bottom side

K/B Connector

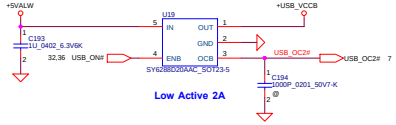


place near KB Conn

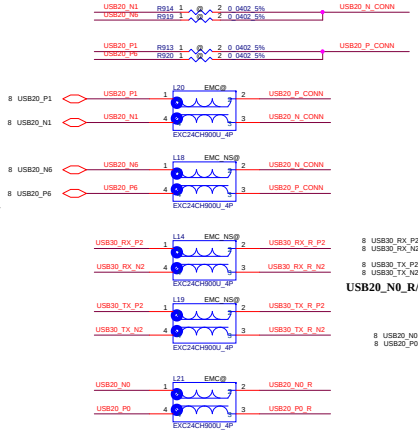
TP/B Connector



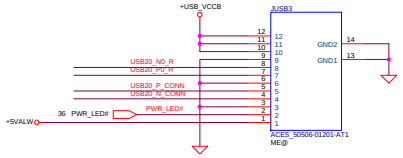
Right Side USB2.0 Port X 2 (USB/B)



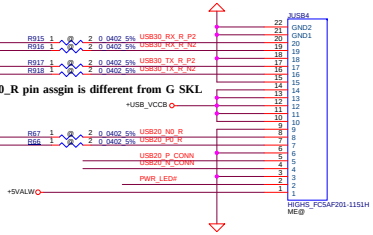
Low Active 2A



USB I/O Connector for G, USB2.0*2

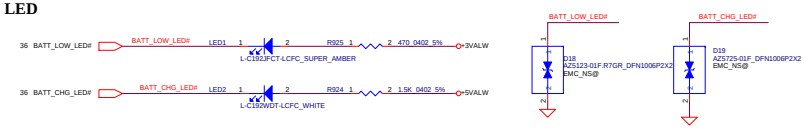


USB20_N0_R/USB20_P0_R pin assgin is different from G SKL

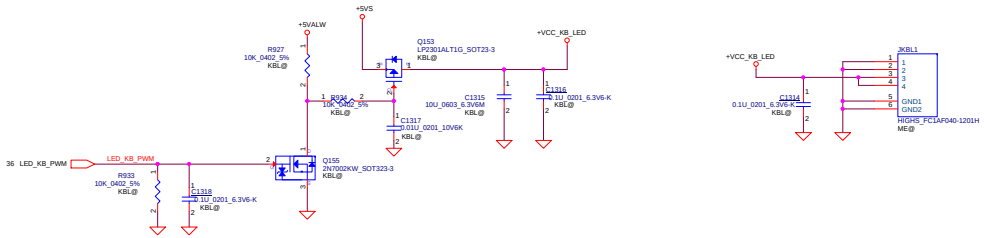


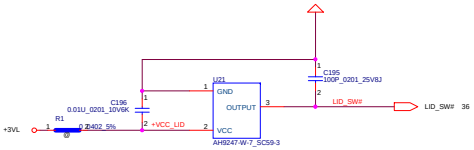
USB I/O Connector for Z, USB2.0*1+USB3.0*1

LED



check LED location and BOM structure when placement and Load BOM, PWR LED and BATT LED have the same location on 14"/15" 02/26





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Title: KBD/PWR/IO/LED/TP Conn.

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Date: Tuesday, April 12, 2016 | Sheet 37 of 51

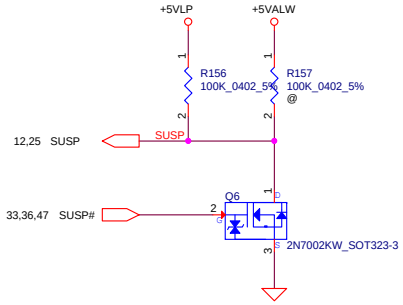
EC need 1.8VS power ready before 3.3VS, chagne C173 from 2200pf to 4700pf

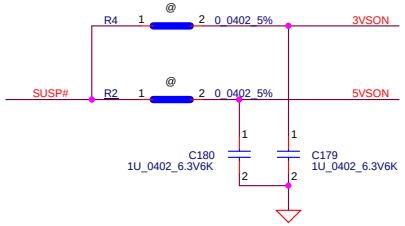
Load Switch

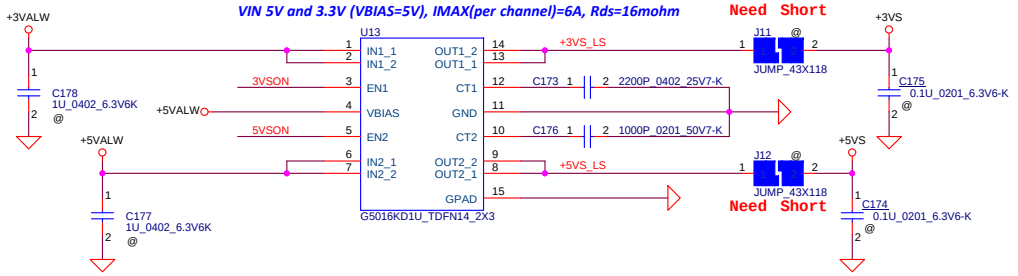
+5VALW To +5VS — **+3VS, C173 --> 5.78ms**

+3VALW To +3VS — **+5VS, C176 --> 1.71ms**

modify load swt ichfro mAPL3523 to G5016KD1UTDFN14P



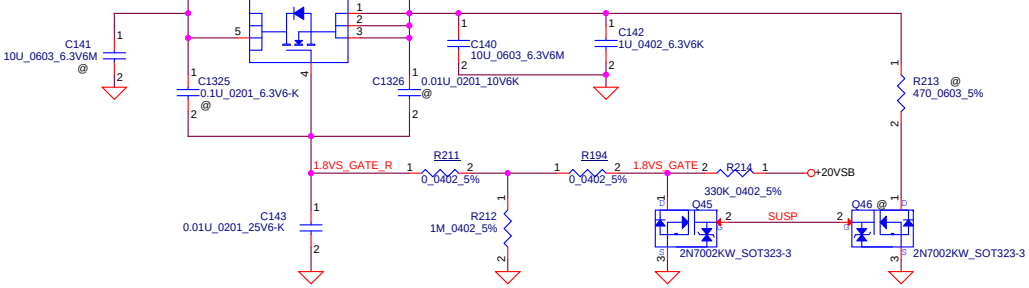




+1.8VALW to +1.8VS

+/- 2% **+/- 5% 1.5A**

AON6414AL
VDS=30V VGS=20V, ID=50A,
Rds=8mohm @ VGS=10V
VGS(th)=2.5V Max

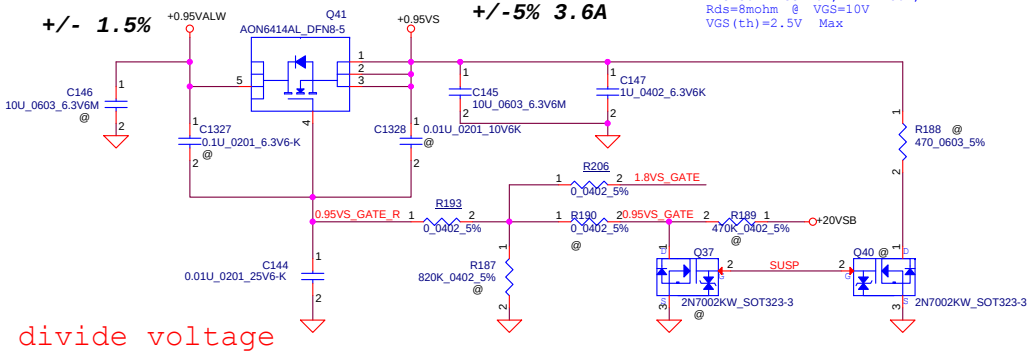


20VSB will change to 6V in DC mode, careful the Res divide voltage

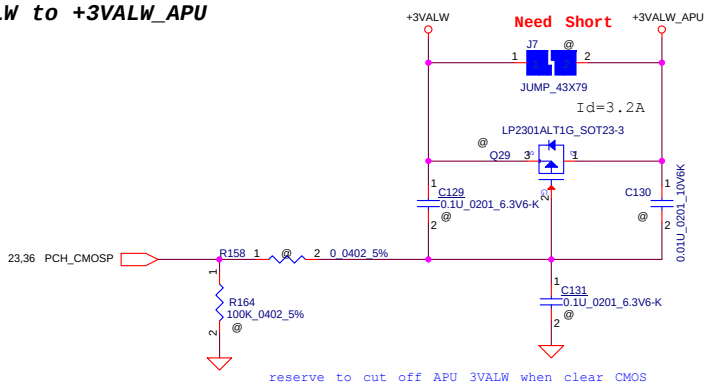
+0.95VALW to +0.95VS

+/- 1.5% **+/-5% 3.6A**

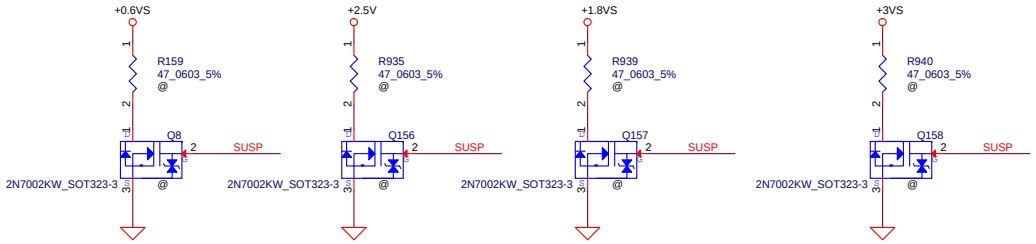
AON6414AL
VDS=30V VGS=20V, ID=50A,
Rds=8mohm @ VGS=10V
VGS(th)=2.5V Max



+3VALW to +3VALW_APU



For DisCharge



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Title: **DC V TO VS INTERFACE**

Size: Custom | Document Number: **CG516** | Rev: 1.0

Date: Tuesday, April 12, 2016 | Sheet 38 of 51

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Title: *Hole*

Size: B | Document Number: **CG516** | Rev: 1.0

Date: Tuesday, April 12, 2016 | Sheet 39 of 51

ZZZ1
PCB CG516 NM-A741 NS-A741/A743/A744
DAZ12300100
PCB_MB

UL1
LAN Chip
SA000074W00
8111H@
LAN Chip

ZZZ3
HDMI Loga
HDMI@
RO00000040J
HDMI Logo

UC2
BRISTOL FM980PADY44AB 2.7G PR 1.0
FX9800P@
SA00007RC10

UC2
BRISTOL AM970PADY44AB 2.5G PR 1.0
A129700P@
SA00007RE10

UC2
BRISTOL AM960PADY44AB 2.4G PR 1.0
A109600P@
SA000007TF00
APU type

ZZZ8
Samsung DRAM
MDS8GX4@
X7611912002

ZZZ9
Micron DRAM
MDM8GX4@
X7611912001
DRAM X76 BOM

UD1 MD_S8G@
K4A8G165WB-BCPB
SA00007DA10

UD2 MD_S8G@
K4A8G165WB-BCPB
SA00007DA10

UD3 MD_S8G@
K4A8G165WB-BCPB
SA00007DA10

UD4 MD_S8G@
K4A8G165WB-BCPB
SA00007DA10

RC257 MD_S8G@
10K_0402_5%
SD028100280

RC264 MD_S8G@
2K_0402_5%
SD028200183
DRAM_Samsung 4G

UD1 MD_M8G@
MT40A512M16HA-083E:A
SA000079F10

UD2 MD_M8G@
MT40A512M16HA-083E:A
SA000079F10

UD3 MD_M8G@
MT40A512M16HA-083E:A
SA000079F10

UD4 MD_M8G@
MT40A512M16HA-083E:A
SA000079F10

RC258 MD_M8G@
2K_0402_5%
SD028200183

RC265 MD_M8G@
10K_0402_5%
SD028100280
DRAM_Micron 4G

DRAM_Hynix 4G

DRAM ID config

Memory Type		BOARD_ID3 AGPIO15 internal pull up 40K	BOARD_ID4 AGPIO13 internal pull up 40K	BOARD_ID5 AGPIO14 internal pull up 40K	BOARD_ID6 AGPIO9 internal pull Low 40K
512Mx16	Samsung K4A8G165WB-BCPB	1 RC257:stuff RC258:NC	0 RC265:NC RC264:stuff		
	Micron MT40A512M16HA-083E:A	0 RC257:NC RC258:stuff	1 RC265:stuff RC264:NC		

ZZZ5
Hynix
H4GX4@
X7610512101

ZZZ6
Samsung
S4GX4@
X7610612101

ZZZ7
MICRON
M4GX4@
X7610612001

UV5 H4G@
H5TC4G63CFR-N0C 4Gb
SA00007DU10

UV6 H4G@
H5TC4G63CFR-N0C 4Gb
SA00007DU10

UV7 H4G@
H5TC4G63CFR-N0C 4Gb
SA00007DU10

UV8 H4G@
H5TC4G63CFR-N0C 4Gb
SA00007DU10

RV70 H4G@
4.75K_0402_1%
SD034475180
VRAM_Hynix_256M*16
000

UV5 M4G@
MT41J256M16LY-091G:N
SA00007QJ00

UV6 M4G@
MT41J256M16LY-091G:N
SA00007QJ00

UV7 M4G@
MT41J256M16LY-091G:N
SA00007QJ00

UV8 M4G@
MT41J256M16LY-091G:N
SA00007QJ00

RV63 M4G@
4.53K_0402_1%
SD034453180

RV70 M4G@
2K_0402_1%
SD034200183
VRAM_Micron_256M*16
010

UV5 S4G@
K4W4G1646E-BC1A 4Gb
SA000063F20

UV6 S4G@
K4W4G1646E-BC1A 4Gb
SA000063F20

UV7 S4G@
K4W4G1646E-BC1A 4Gb
SA000063F20

UV8 S4G@
K4W4G1646E-BC1A 4Gb
SA000063F20

RV63 S4G@
8.45K_0402_1%
SD000011R00

RV70 S4G@
2K_0402_1%
SD034200183
VRAM_Samsung_256M*16
001

VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
128Mx16	NA	100	4.53K	4.99K
	NA	111	4.75K	NC
	NA	110	3.4K	10K
256Mx16	Hynix H5TC4G63CFR-N0C 4Gb 900(1G)	000	NC	4.75K
	Micron MT41J256M16LY-091G:N 4Gb 900(1G)	010	4.53K	2K
	Samsung K4W4G1646E-BC1A 4Gb 900(1G)	001	8.45K	2K

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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Title
Virtual symbol

Size: Custom
Document Number: CG412
Rev: 0.1
Date: Tuesday, April 12, 2016
Sheet 40 of 51

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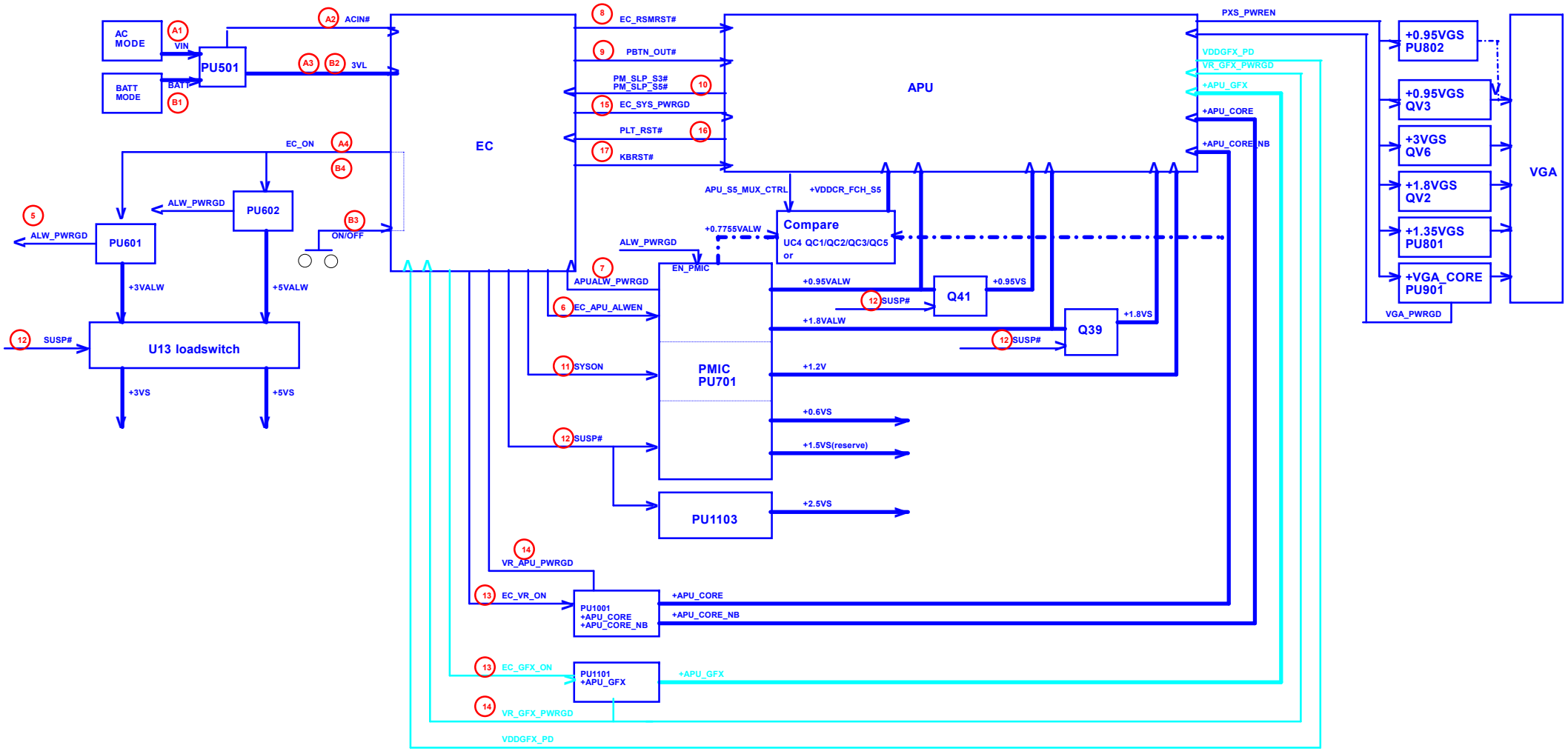

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

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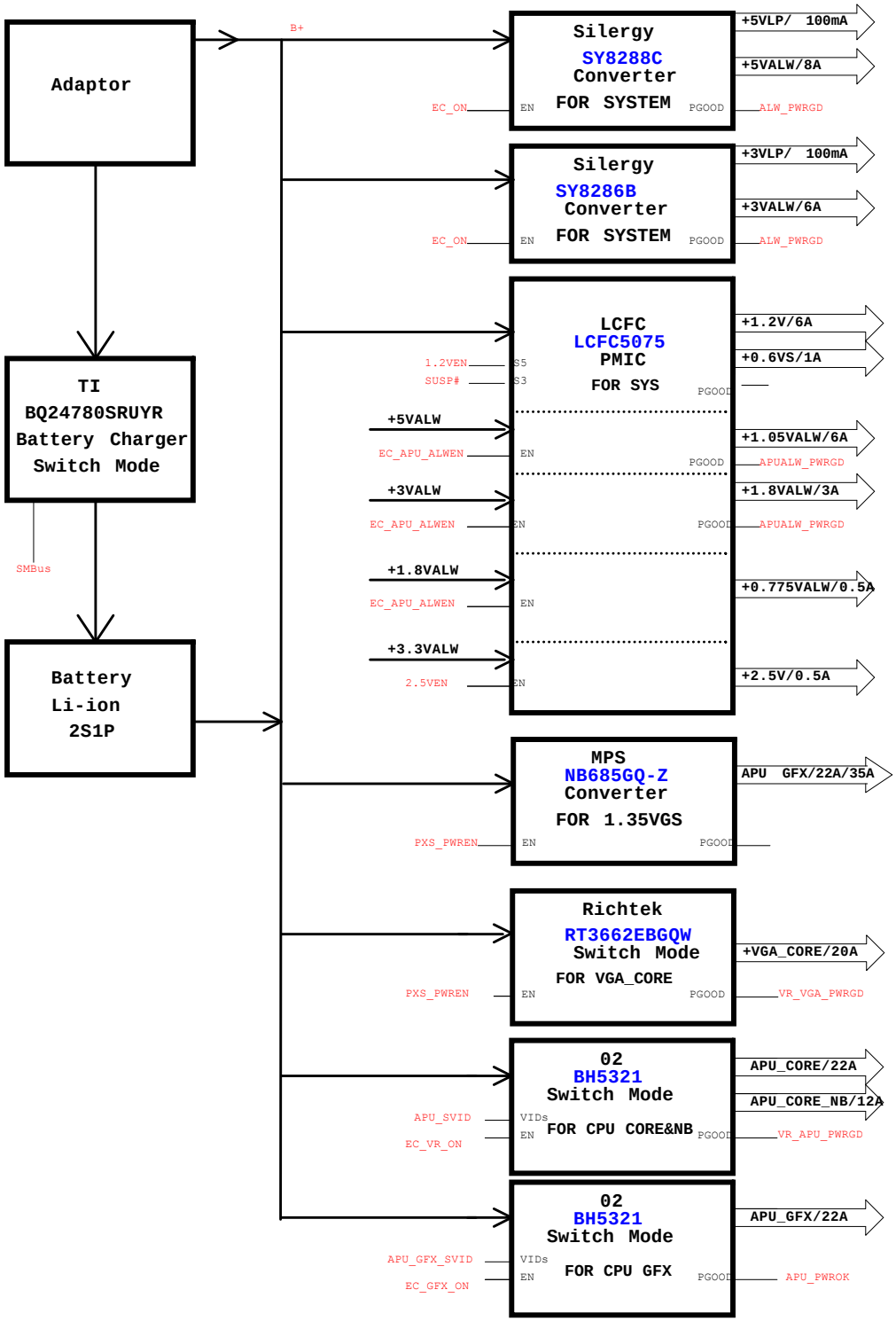
Title: *Power sequence Block*

Size: Custom | Document Number: CG516 | Rev: 1.0

Date: Tuesday, April 12, 2016 | Sheet 41 of 51



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

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Title: **Power Diagram**

Size	Document Number	Rev
Custom	CG516	1.0

Date: Tuesday, April 12, 2016 Sheet 42 of 51

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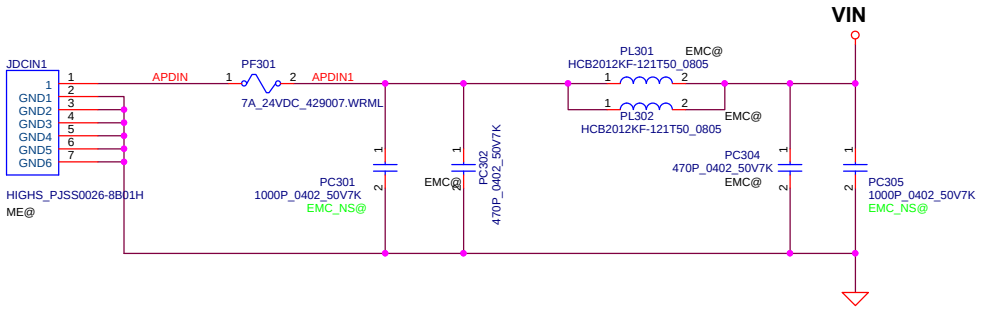

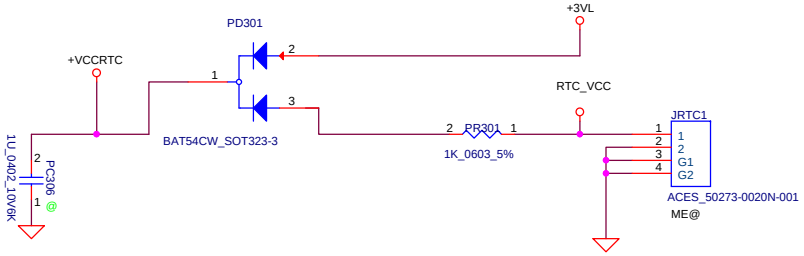

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

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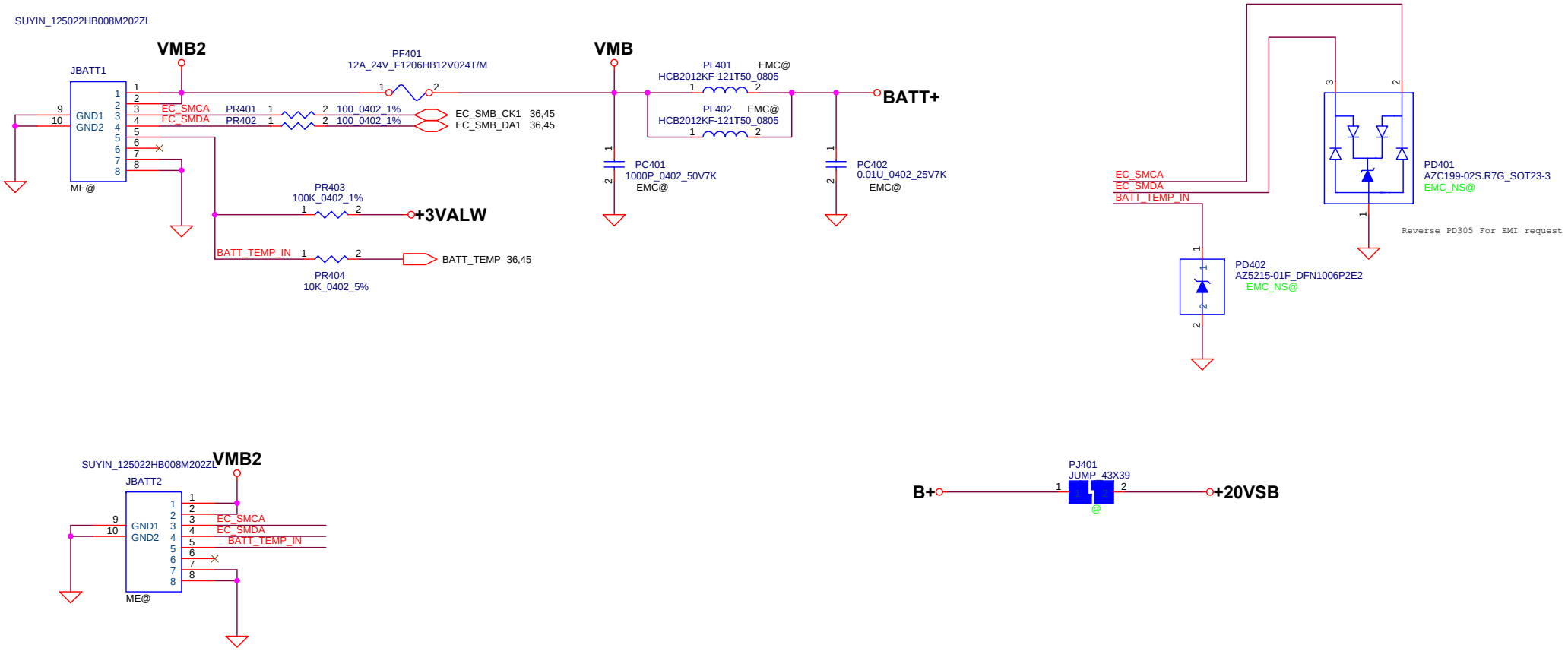
Title
DCIN / RTC

Size: Custom
Document Number: **CG516**
Rev: 1.0
Date: Tuesday, April 12, 2016
Sheet 43 of 51



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

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Title: **BATTERY CONN/OTP**

Size: B | Document Number: **CG516** | Rev: 1.0

Date: Tuesday, April 12, 2016 | Sheet 44 of 51

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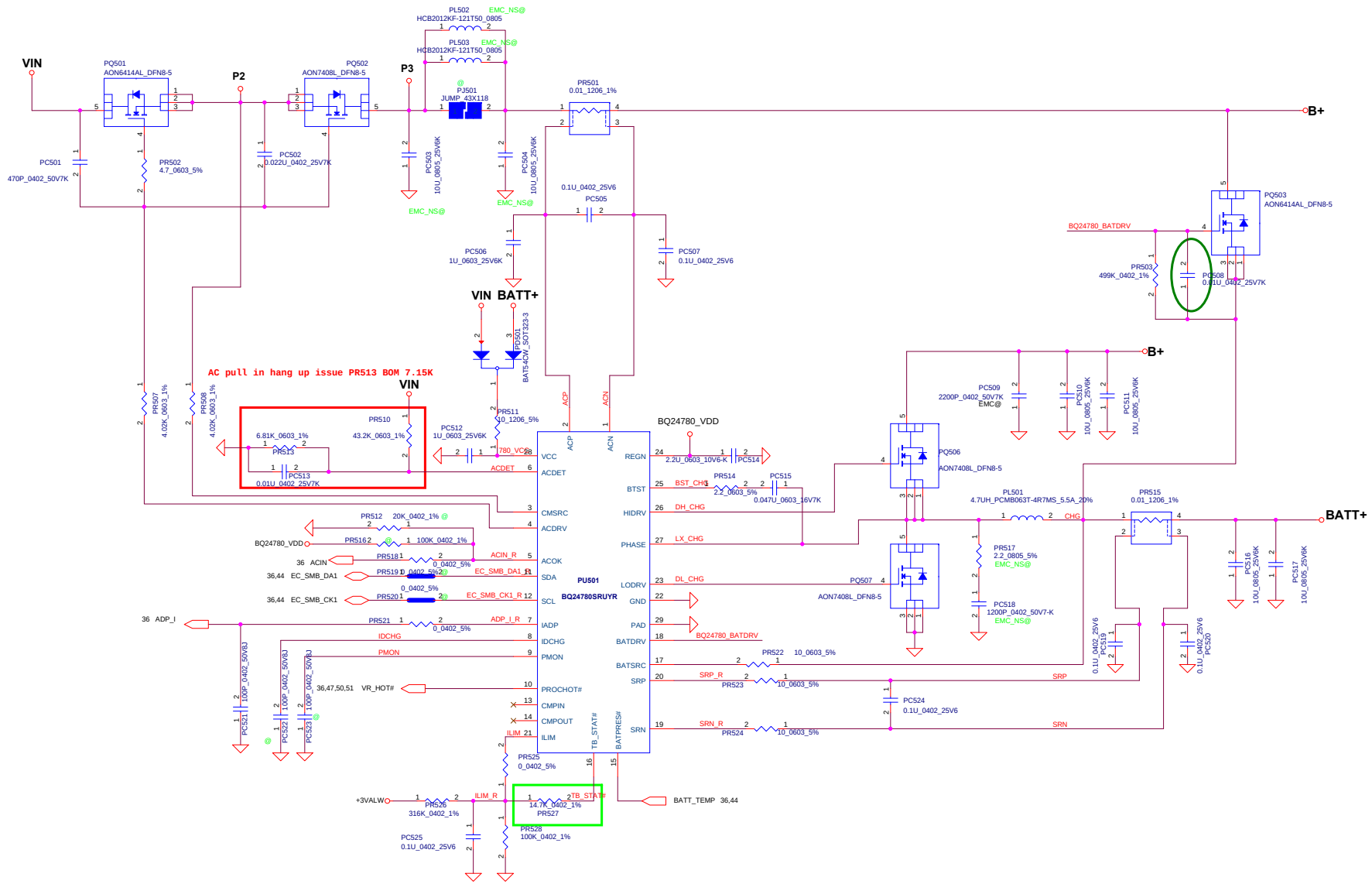

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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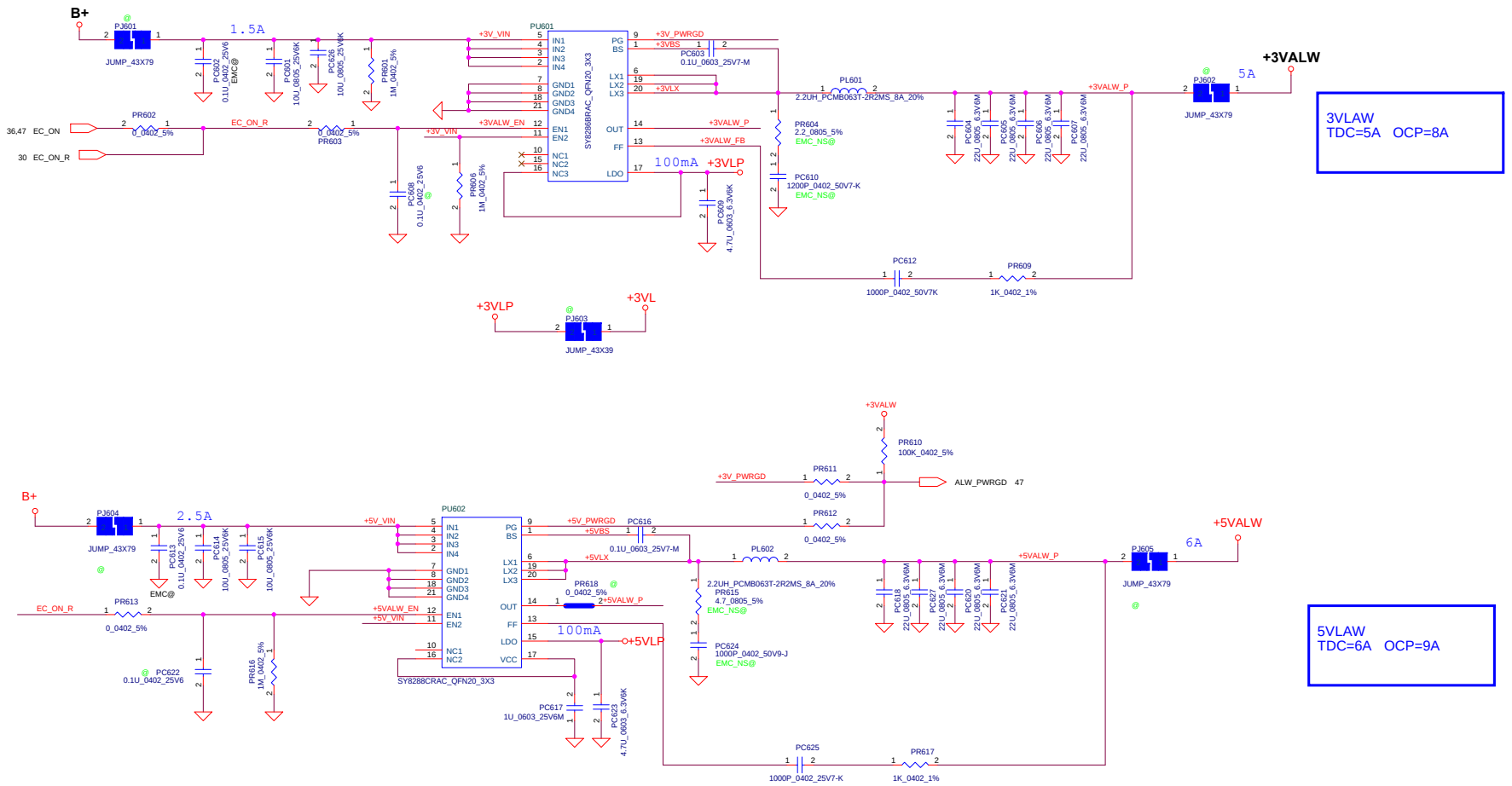
Title: CHARGER

Size: C | Document Number: CG516 | Rev: 1.0

Date: Tuesday, April 12, 2016 | Sheet 45 of 51



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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Title: **PWR_3VALW/5VALW**

Size	Document Number	Rev
C	CG516	1.0

Date: Tuesday, April 12, 2016 Sheet 46 of 51

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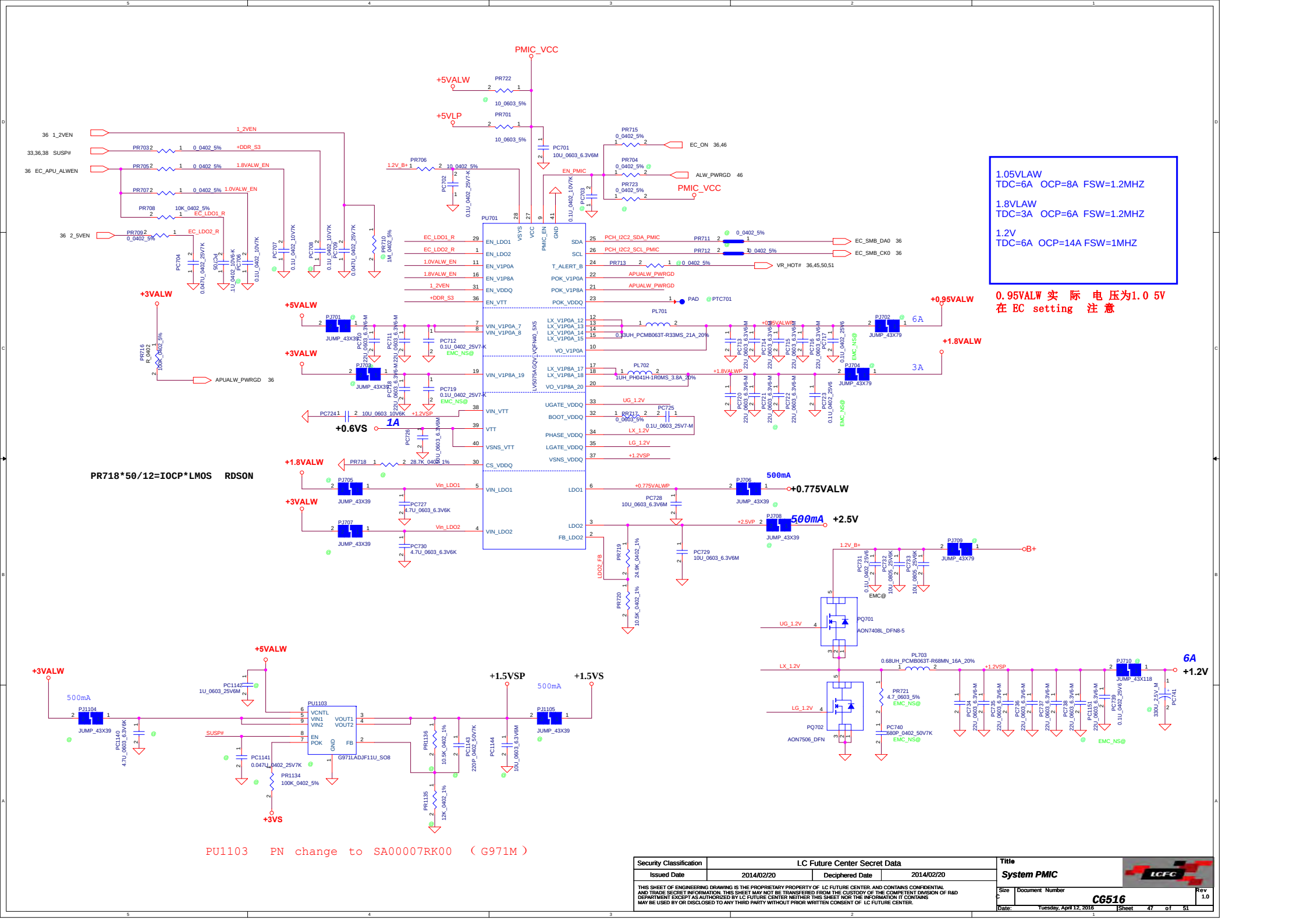

Security Classification	LC Future Center Secret Data		
Issued Date	2014/02/20	Deciphered Date	2014/02/20

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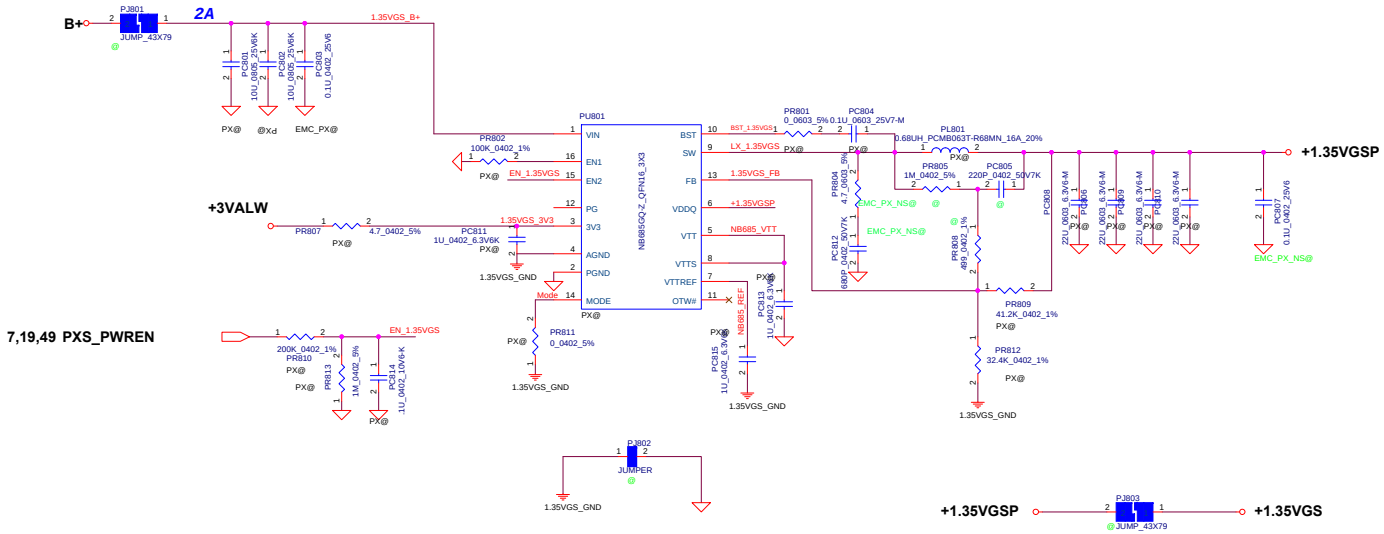
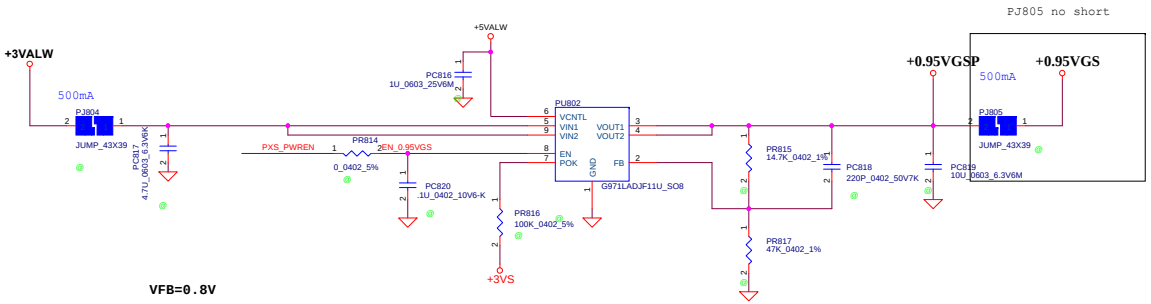
Title: System PMIC

Size: C | Document Number: CG516 | Rev: 1.0

Date: Tuesday, April 12, 2016 | Sheet 47 of 51





PU802 PN change to SA00007RK00 (G971M)

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

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Title: 1.35VGS

Size: Custom | Document Number: CG516 | Rev: 1.0

Date: Tuesday, April 12, 2016 | Sheet 48 of 51

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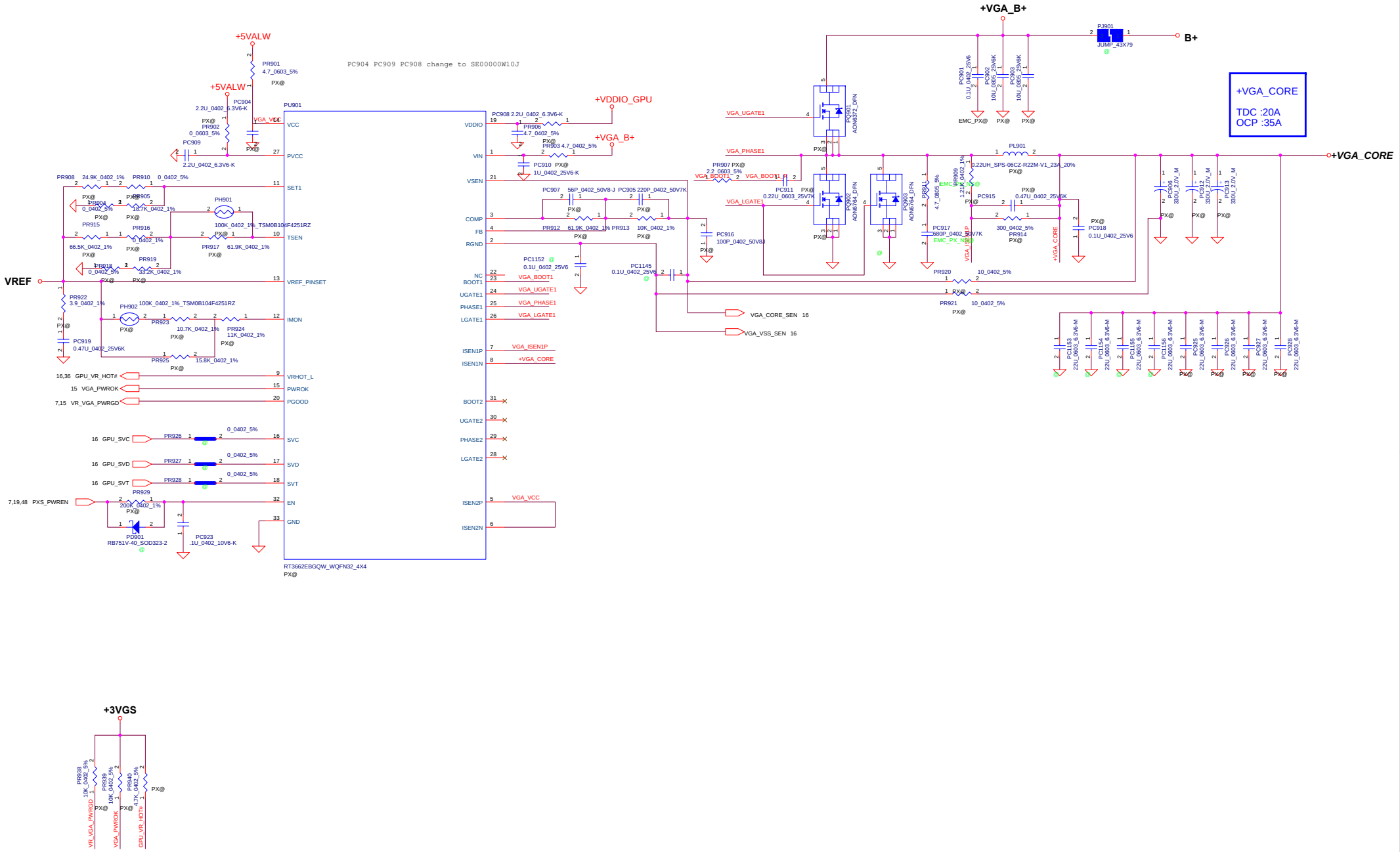

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

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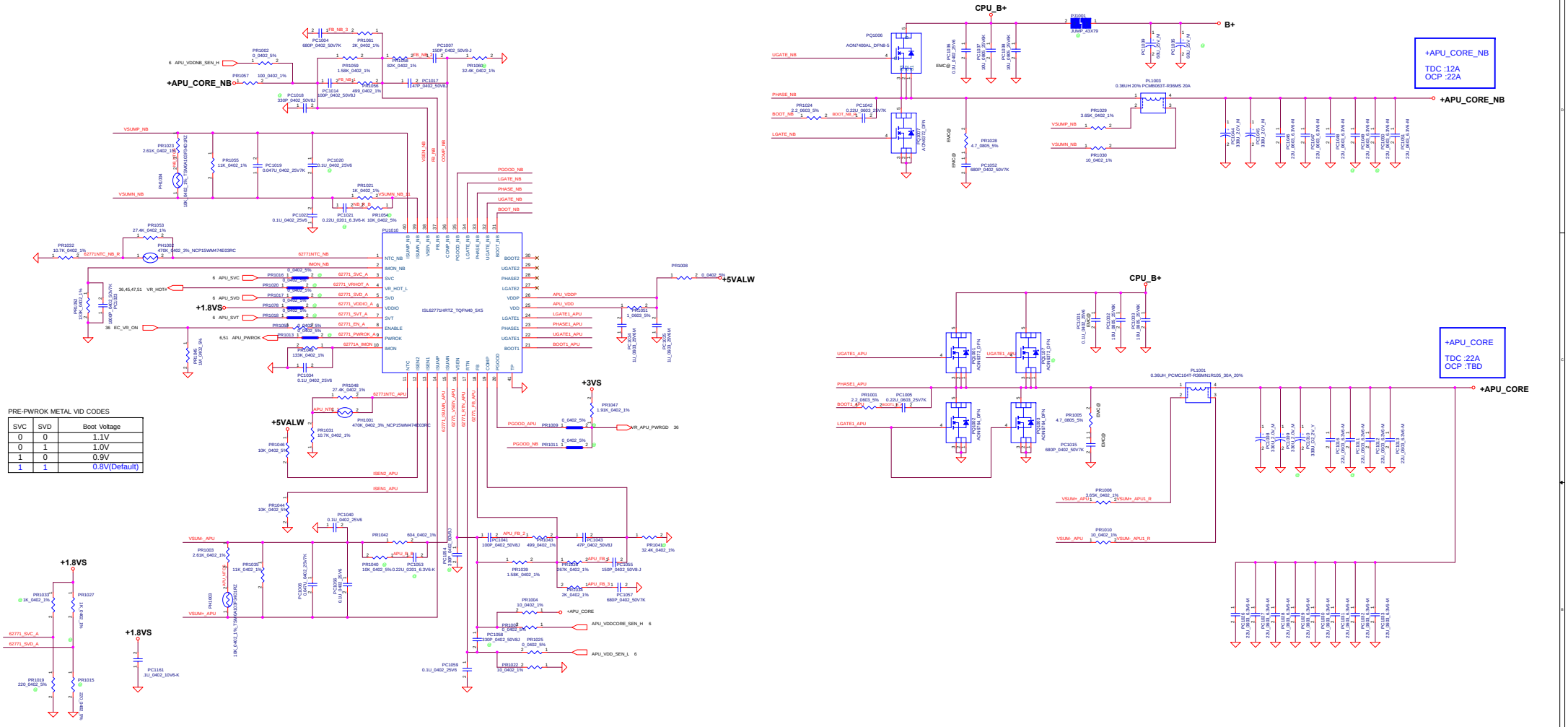
Title: +VGA_CORE

Size: Custom | Document Number: CG516 | Rev: 1.0

Date: Tuesday, April 12, 2016 | Sheet 49 of 51



PRE-PWROK METAL VID CODES

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V(Default)

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

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Title: PWR_CPU Core

Size: A | Document Number: CG516 | Rev: 1.0

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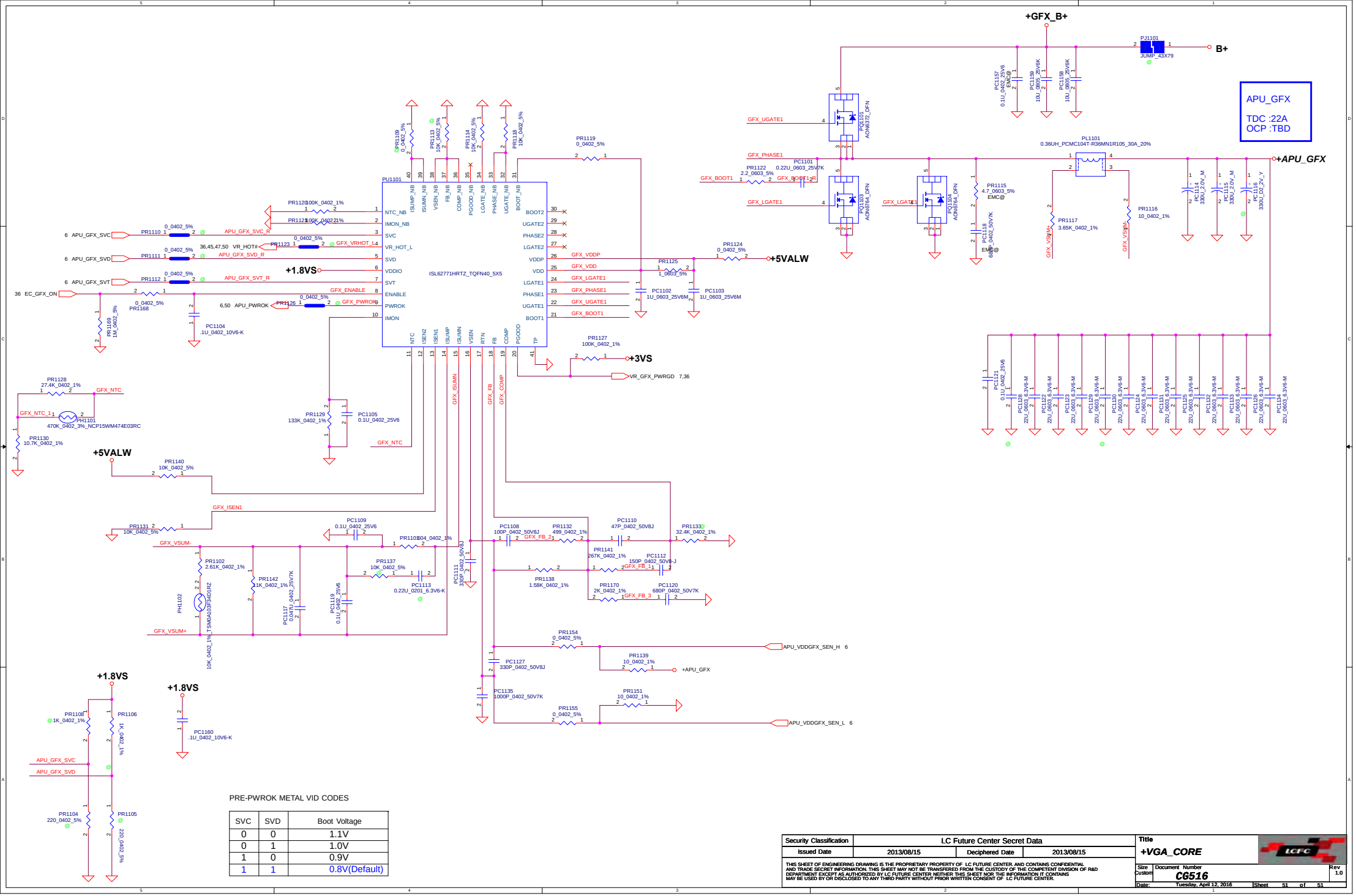

PRE-PWROK METAL VID CODES

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V(Default)

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

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Title: +VGA_CORE

Size: Custom | Document Number: CG516 | Rev: 1.0

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